COMBINATIONAL ICs

- REPRESENTATION OF BINARY VARIABLES AT THE PHYSICAL LEVEL
- BASIC SWITCH. STRUCTURE OF GATES AND THEIR OPERATION
- REALIZATION OF GATES USING CMOS CIRCUITS
- CHARACTERISTICS OF CIRCUITS: LOAD FACTORS AND FANOUT FACTORS, PROPAGATION DELAYS, TRANSITION TIMES, AND EFFECT OF LOAD
- THREE-STATE GATES (DRIVERS) AND BUSES
- NOISE AND NOISE MARGINS
- EVOLUTION OF ICs. VLSI CIRCUIT-LEVEL DESIGN STYLES
- PACKAGING LEVELS: CHIPS, BOARDS AND CABINETS.

REPRESENTATION OF BINARY VARIABLES

- REPRESENTATION OF 0 AND 1 BY ELECTRICAL SIGNALS
  - VOLTAGES
  - CURRENTS
  - ELECTRICAL CHARGES
- REALIZATION OF CIRCUITS THAT OPERATE ON THESE SIGNALS TO IMPLEMENT DESIRED SWITCHING FUNCTIONS

TYPICAL VALUES FOR A 3.3V CMOS TECHNOLOGY

V_{Hmax}	3.3V	V_{Lmax}	0.8V
V_{Hmin}	2.0V	V_{Lmin}	0.0V

VOLTAGE REGIONS

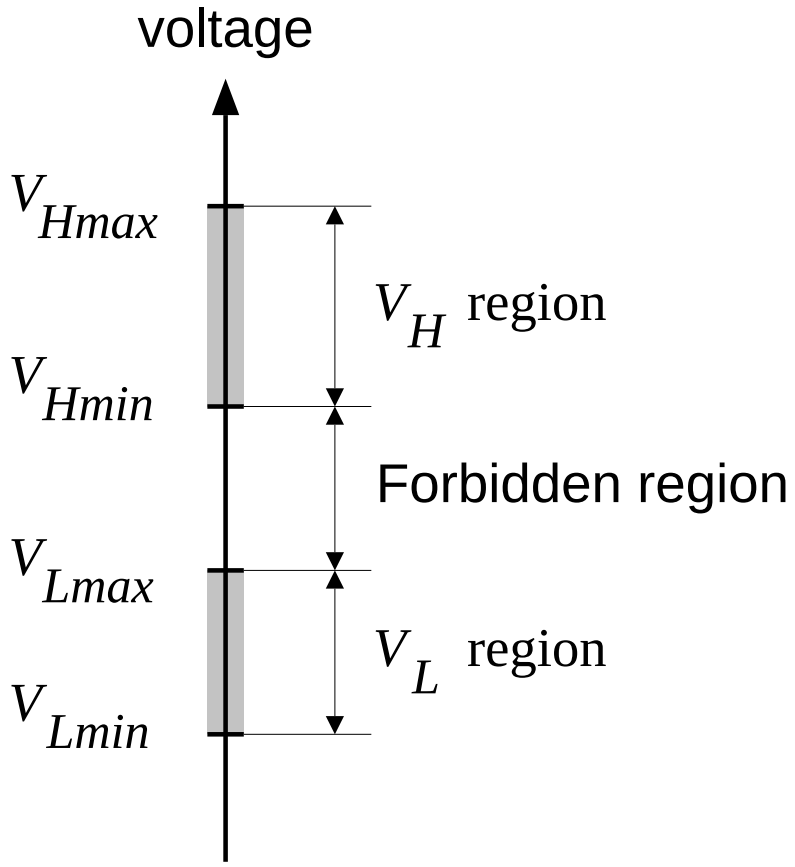
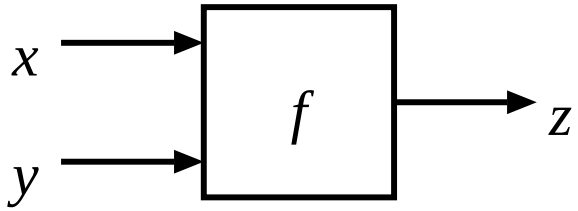


Figure 3.1: VOLTAGE REGIONS.

POSITIVE AND NEGATIVE LOGIC



POSITIVE LOGIC

$V_H \longleftrightarrow 1$

$V_L \longleftrightarrow 0$

NEGATIVE LOGIC

$V_H \longleftrightarrow 0$

$V_L \longleftrightarrow 1$

Input voltages		Output voltage	Positive logic			Negative logic		
x	y	z	x	y	z	x	y	z
V_L	V_L	V_L	0	0	0	1	1	1
V_L	V_H	V_L	0	1	0	1	0	1
V_H	V_L	V_L	1	0	0	0	1	1
V_H	V_H	V_H	1	1	1	0	0	0
			$f = \text{AND}$			$f = \text{OR}$		

SWITCH AND MOS TRANSISTORS

N-TYPE:

OPEN (OFF) if $V_{CA} < V_{Tn}$

CLOSED (ON) if $V_{CA} > V_{Tn}$

V_{Tn} – THE THRESHOLD VOLTAGE FOR N-TYPE SWITCH

P-TYPE:

OPEN (OFF) if $V_{BC} < V_{Tp}$

CLOSED (ON) if $V_{BC} > V_{Tp}$

V_{Tp} – THE THRESHOLD VOLTAGE FOR P-TYPE SWITCH

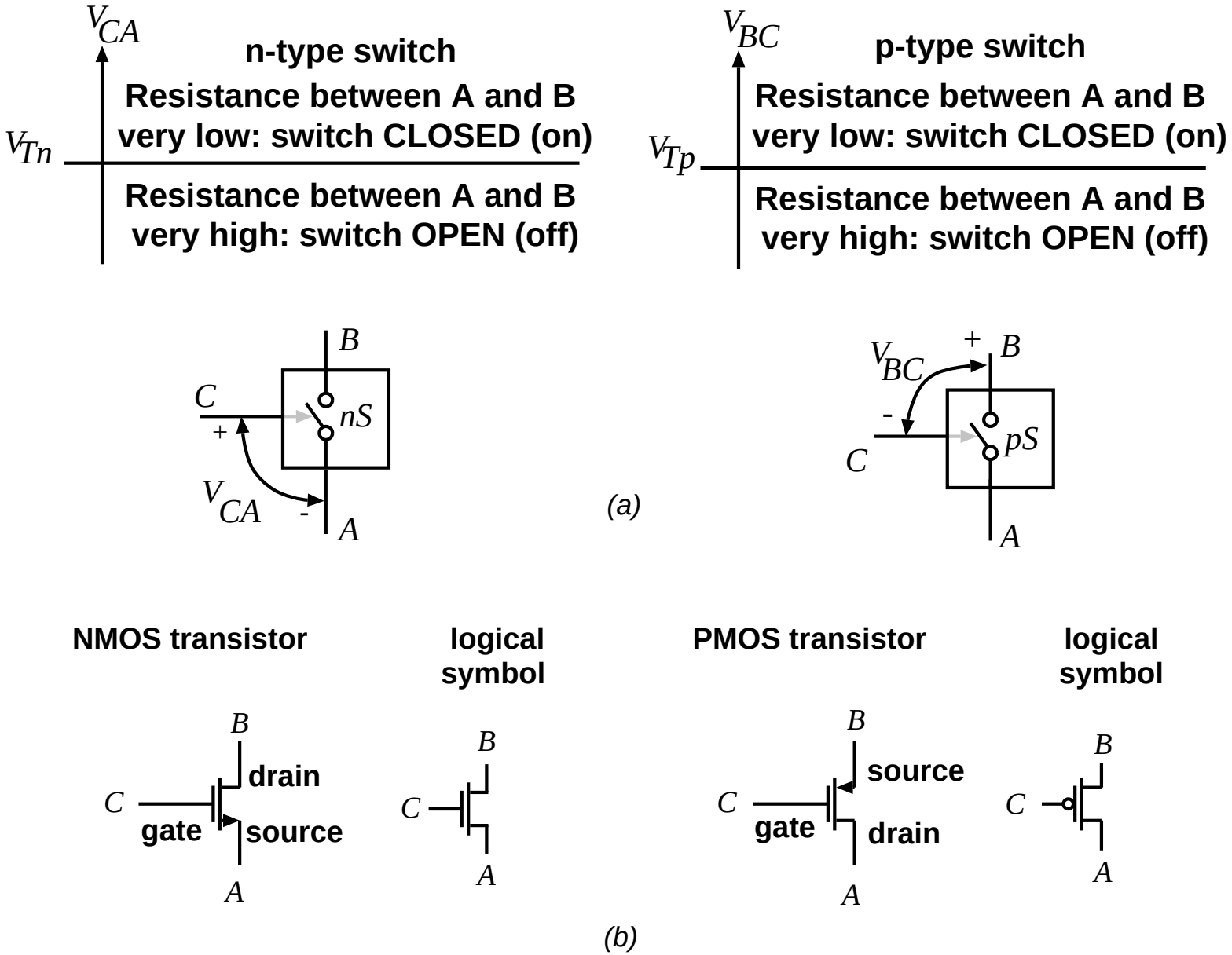


Figure 3.3: a) N-TYPE AND P-TYPE CONTROLLED SWITCHES. b) nMOS AND pMOS TRANSISTORS.

CMOS NOT GATE

- COMPLEMENTARY MOS CIRCUIT

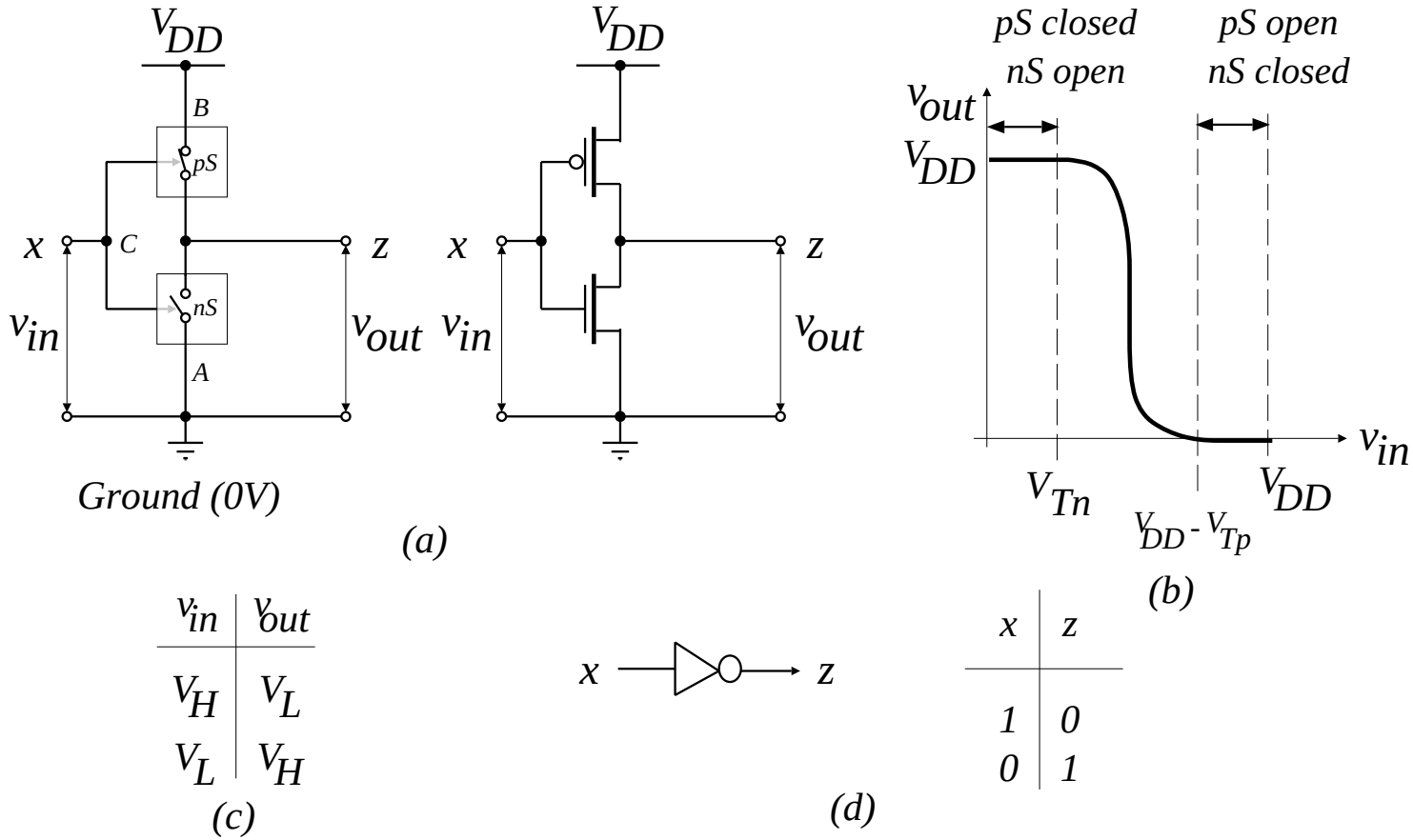


Figure 3.4: CIRCUIT, I/O CHARACTERISTIC, AND SYMBOL

OPERATION OF NOT GATE

$V_{BC} = V_{DD} - v_{in}$ $(V_{DD} = V_{BC} + v_{in})$

1. $v_{in} < V_{Tn} \implies V_{CA} < V_{Tn}$

   $\implies$ N-SWITCH OPEN

   If $V_{DD} > V_{Tn} + V_{Tp}$ then $V_{BC} > V_{Tp}$

   $\implies$ P-SWITCH CLOSED AND $v_{out} = V_{DD}$

2. $v_{in} > V_{DD} - V_{Tp} \implies V_{BC} < V_{Tp}$

   $\implies$ P-SWITCH IS OPEN

   If $V_{DD} > V_{Tn} + V_{Tp}$ then $V_{CA} > V_{Tn}$

   $\implies$ N-SWITCH IS CLOSED AND $v_{out} = 0$

CIRCUIT OPERATES AS NOT IF

$$V_{Lmax} < V_{Tn}, \quad V_{Hmin} > V_{DD} - V_{Tp}$$
$$V_{DD} > V_{Tn} + V_{Tp}$$

NAND and NOR GATES

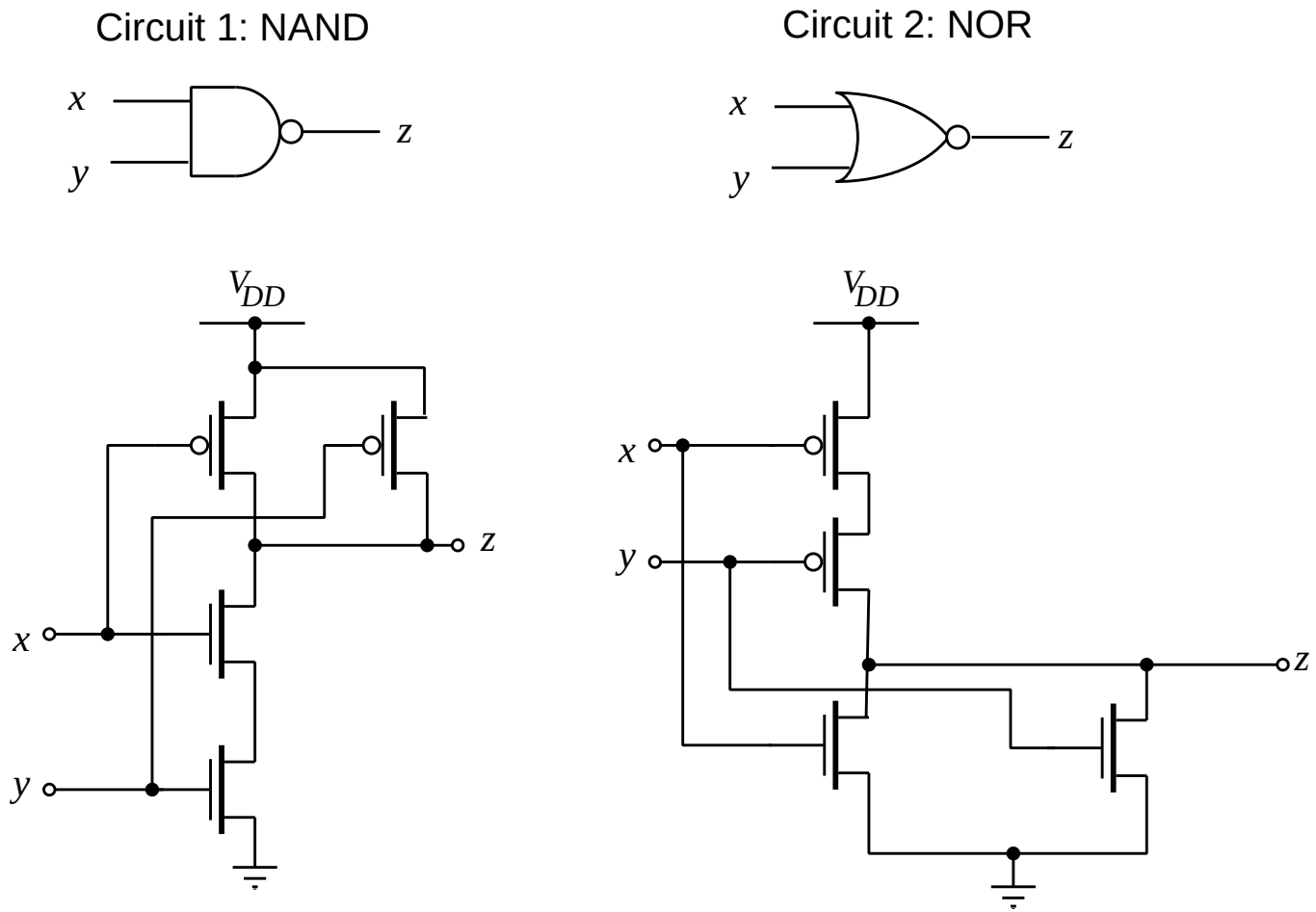


Figure 3.5: CIRCUITS FOR NAND and NOR GATES.

NAND and NOR GATES (cont.)

		Circuit 1	Circuit 2
x	y	z	z
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	0

AND and OR GATES

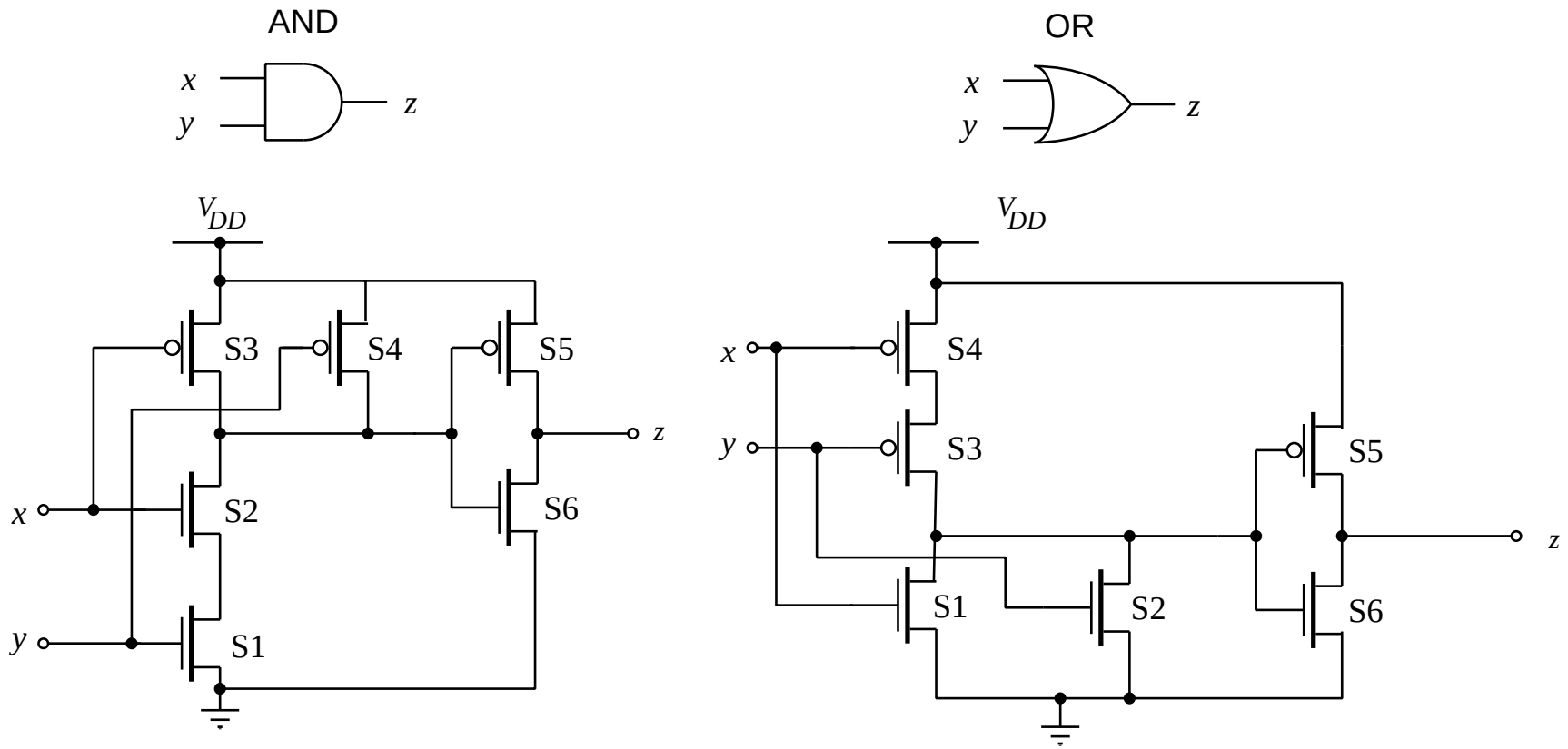
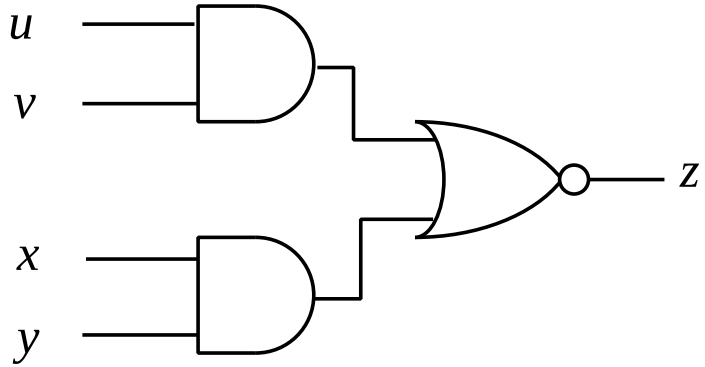


Figure 3.6: CIRCUITS FOR AND and OR GATES.

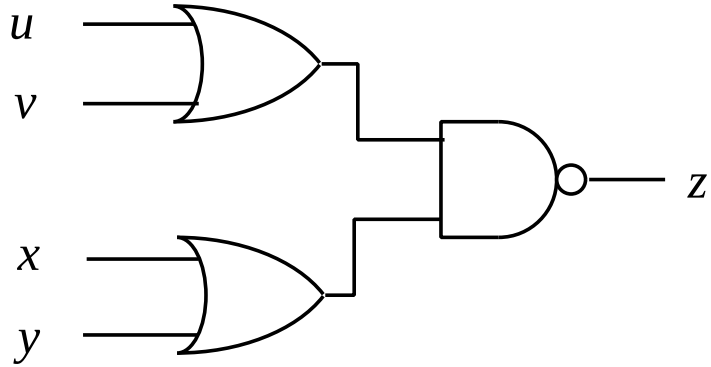
COMPLEX GATES

AND-OR-INVERT (AOI)



$z = (uv + xy)'$

OR-AND-INVERT (OAI)



$z = [(u+v)(x+y)]'$

Figure 3.7: COMPLEX GATES.

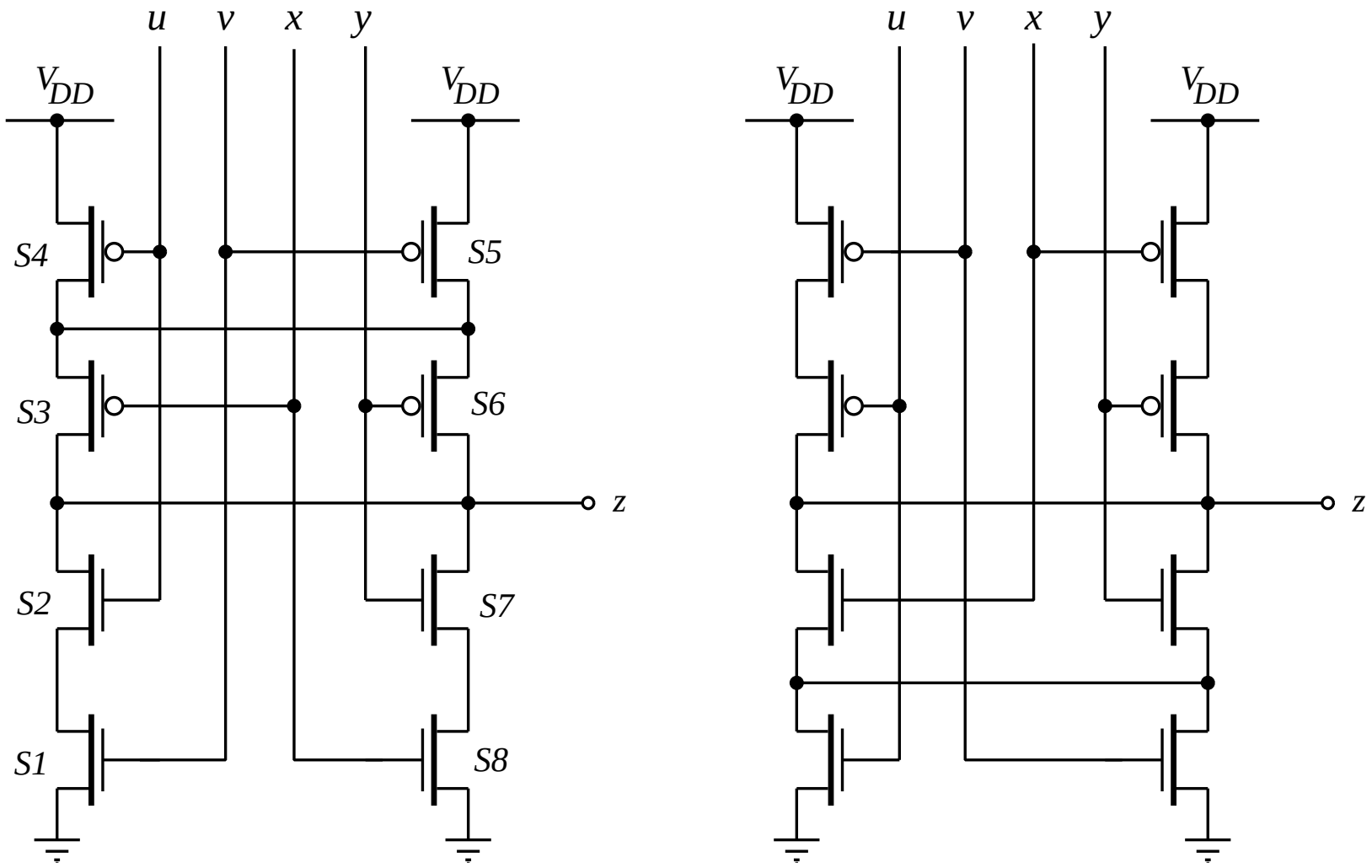
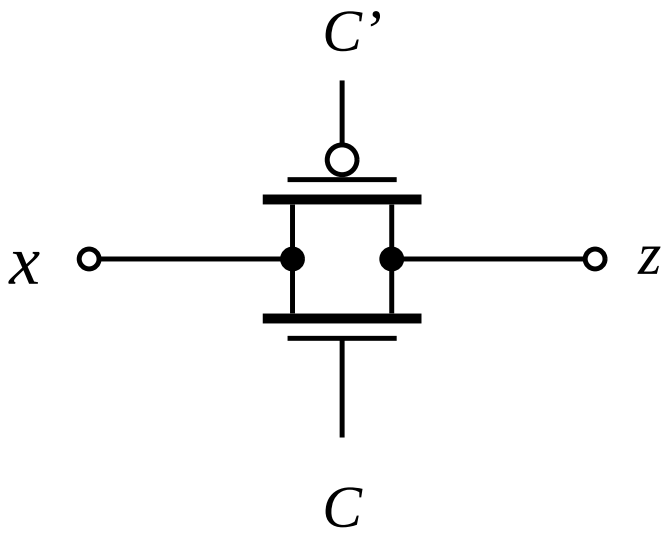


Figure 3.7: EXAMPLES OF COMPLEX GATES.

TRANSMISSION GATE



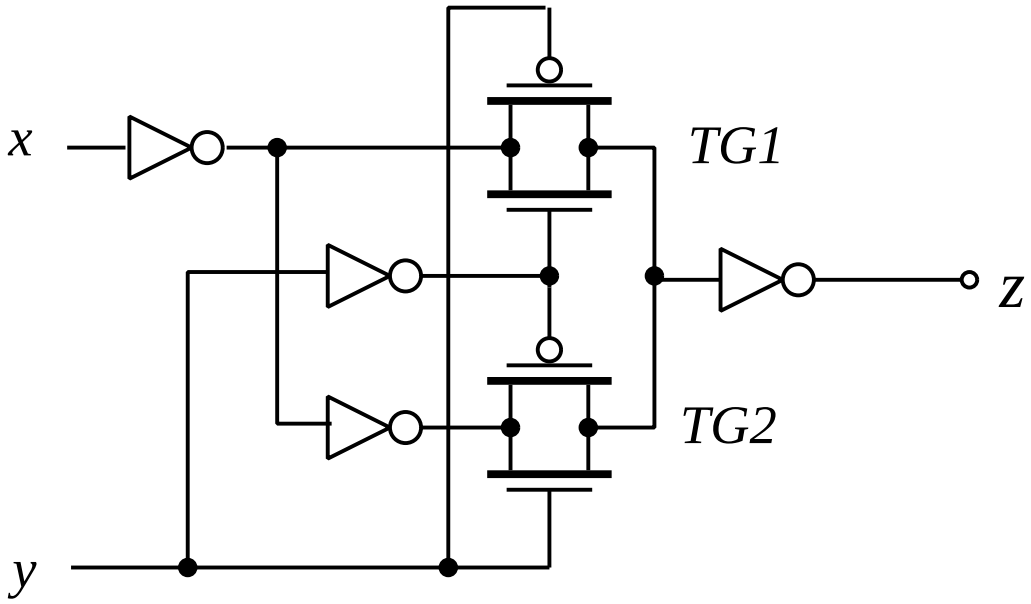
C	n-switch	p-switch	z
0	off	off	Z
1	on	on	x

Z - high impedance state

(a)

Figure 3.8: a) TRANSMISSION GATE

XOR WITH TRANSMISSION GATES



(b)

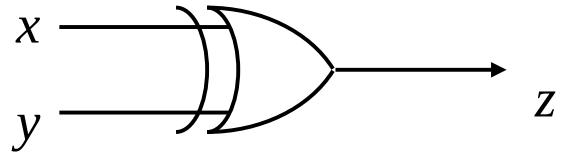
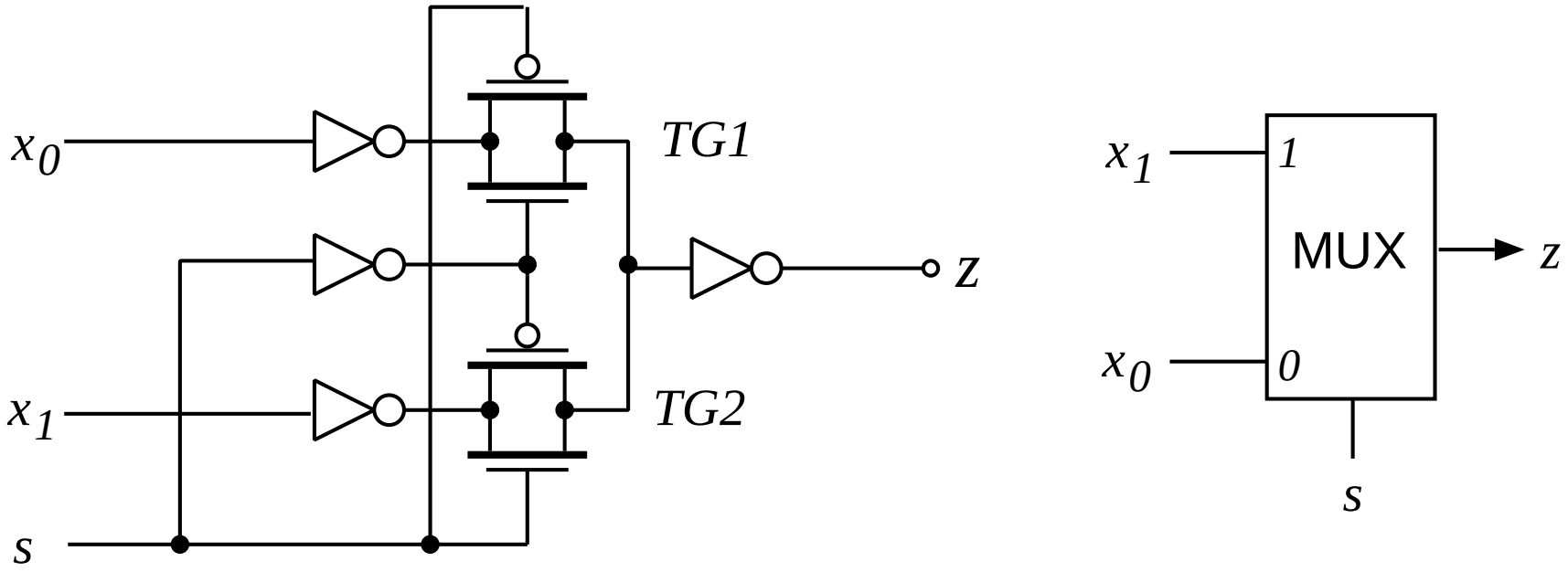


Figure 3.8: b) XOR GATE

y	$TG1$	$TG2$	z
0	ON	OFF	x
1	OFF	ON	x'

MUX WITH TRANSMISSION GATES



(c)

Figure 3.8: c) 2-INPUT MUX.

$$z = \text{MUX}(x_1, x_0, s) = x_1 s + x_0 s'$$

s	$TG1$	$TG2$	z
0	ON	OFF	x_0
1	OFF	ON	x_1

TIMING PARAMETERS

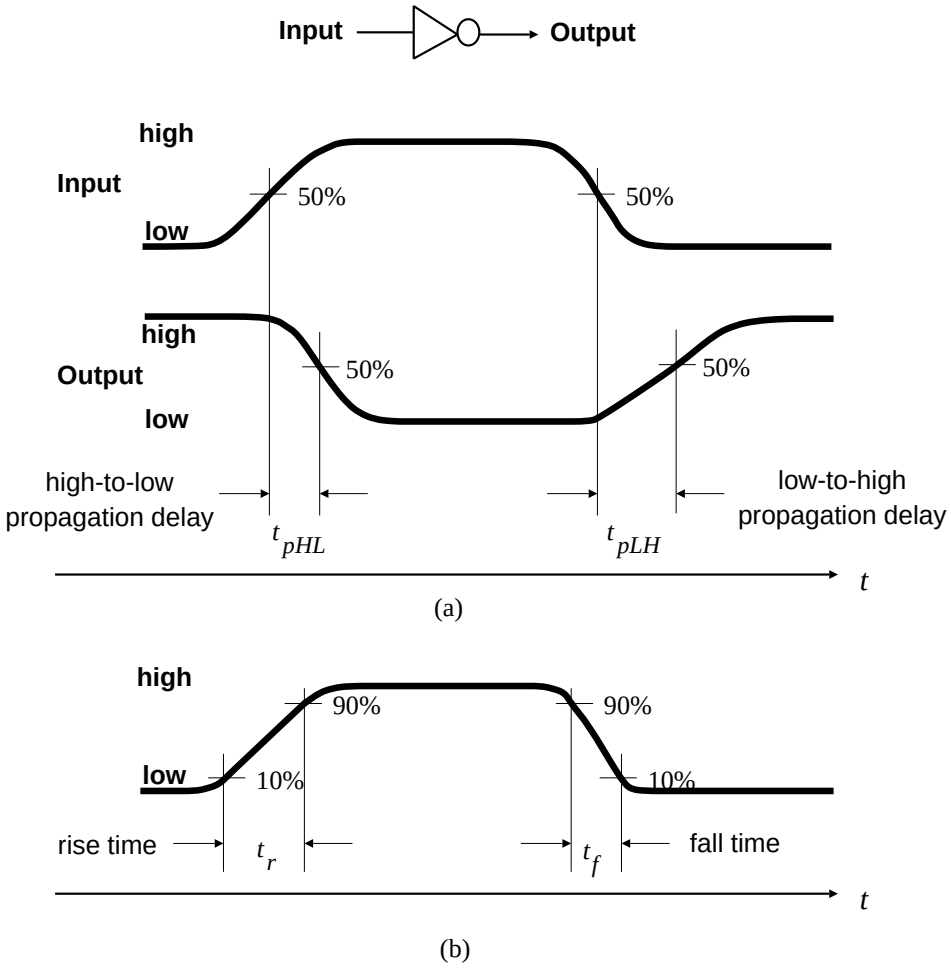


Figure 3.9: a) PROPAGATION DELAY. b) RISE AND FALL TIMES.

EFFECT OF LOAD

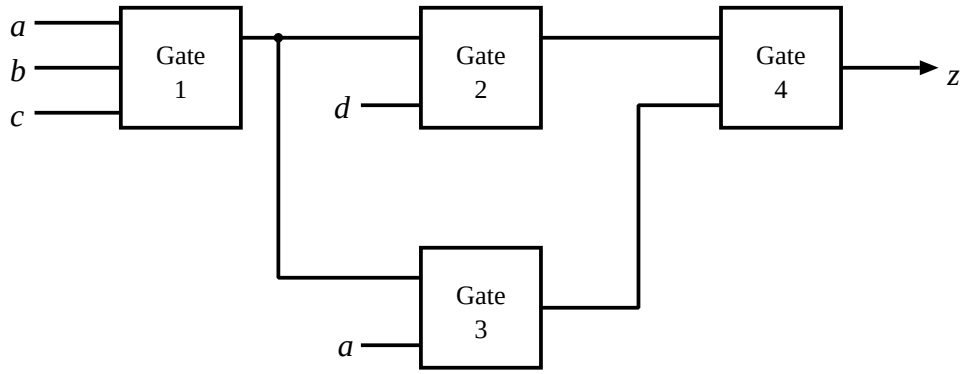


Figure 3.10: A GATE NETWORK

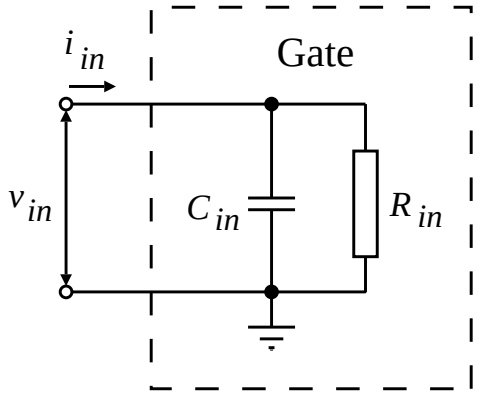


Figure 3.11: EQUIVALENT CIRCUIT FOR GATE INPUT.

EFFECT OF LOAD ON PROPAGATION DELAY

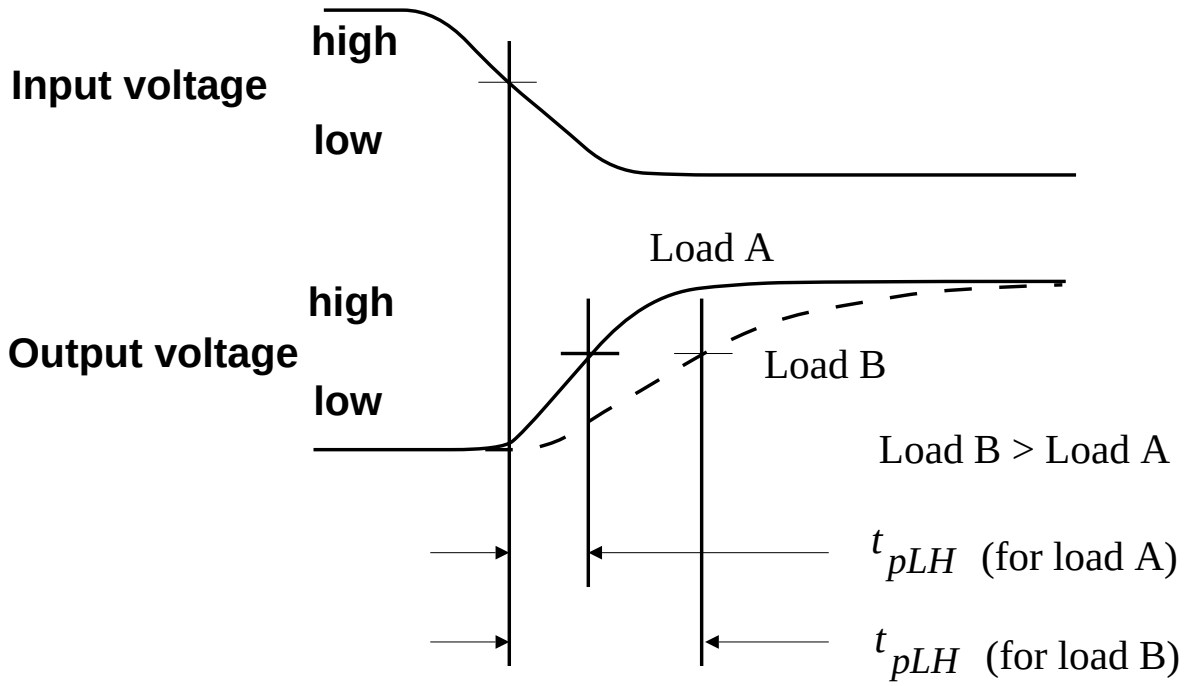


Figure 3.12: EFFECT OF LOAD ON PROPAGATION DELAY.

LOAD FACTOR AND TOTAL LOAD

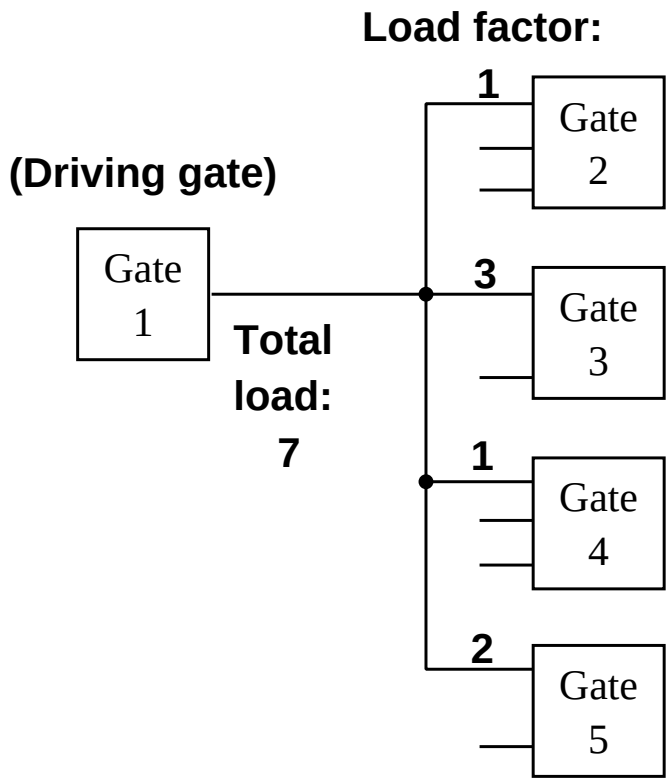


Figure 3.13: OUTPUT LOAD OF GATE 1.

VOLTAGE VARIATIONS AND NOISE MARGINS

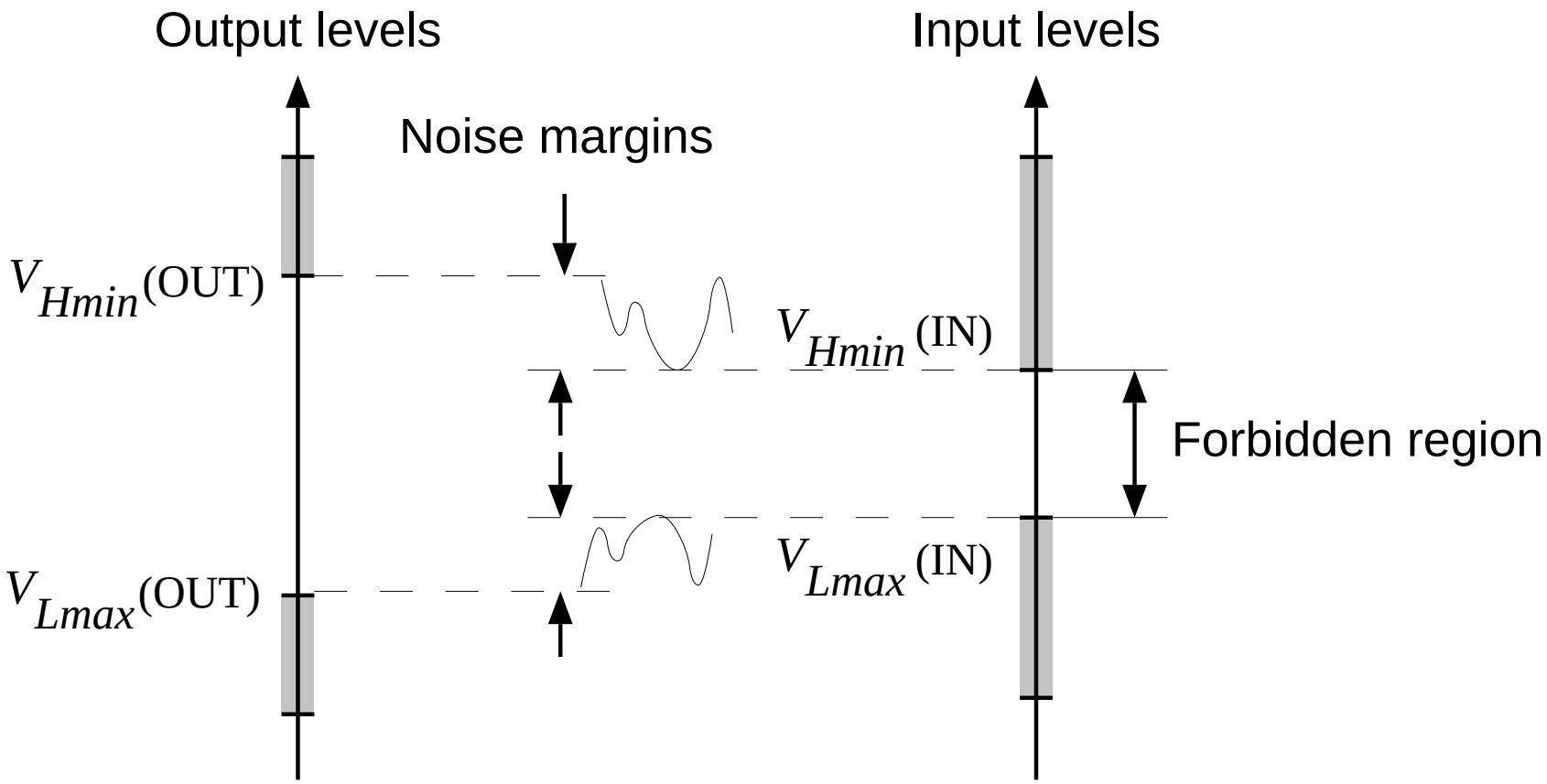


Figure 3.14: NOISE MARGINS.

NOISE MARGINS: EXAMPLE

LEVELS			NOISE MARGIN
HIGH	$V_{Hmin}(\text{OUT})$	2.4 V	0.4 V
	$V_{Hmin}(\text{IN})$	2.0 V	
LOW	$V_{Lmax}(\text{OUT})$	0.4 V	0.4 V
	$V_{Lmax}(\text{IN})$	0.8 V	

CONNECTING MODULES TO A BUS

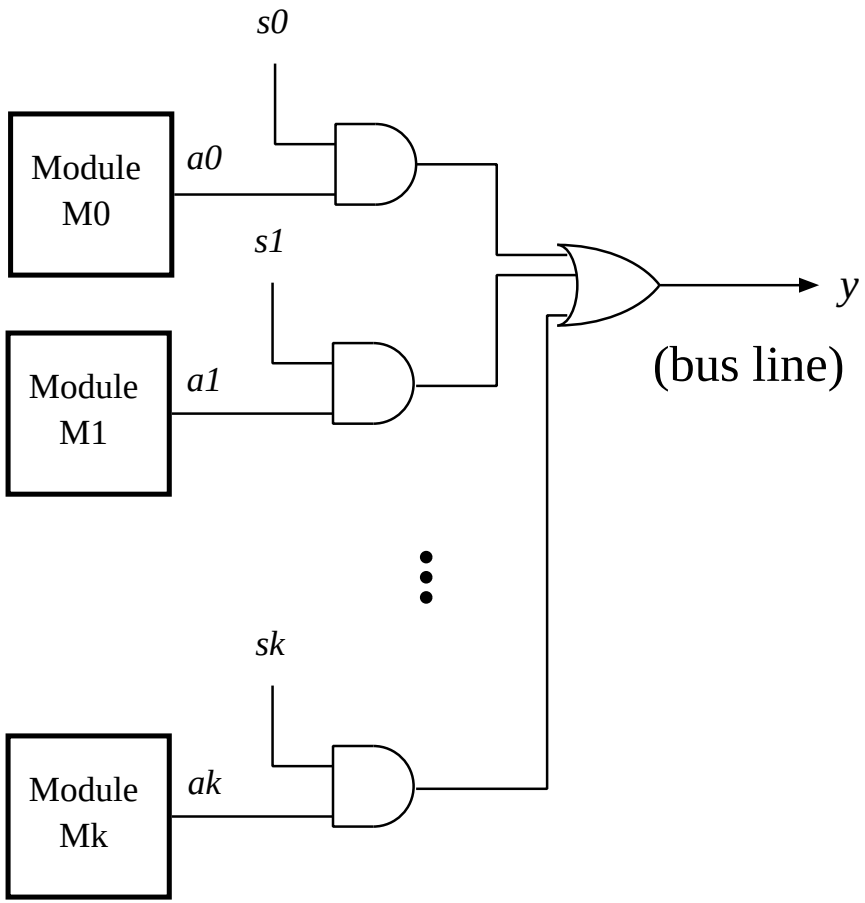
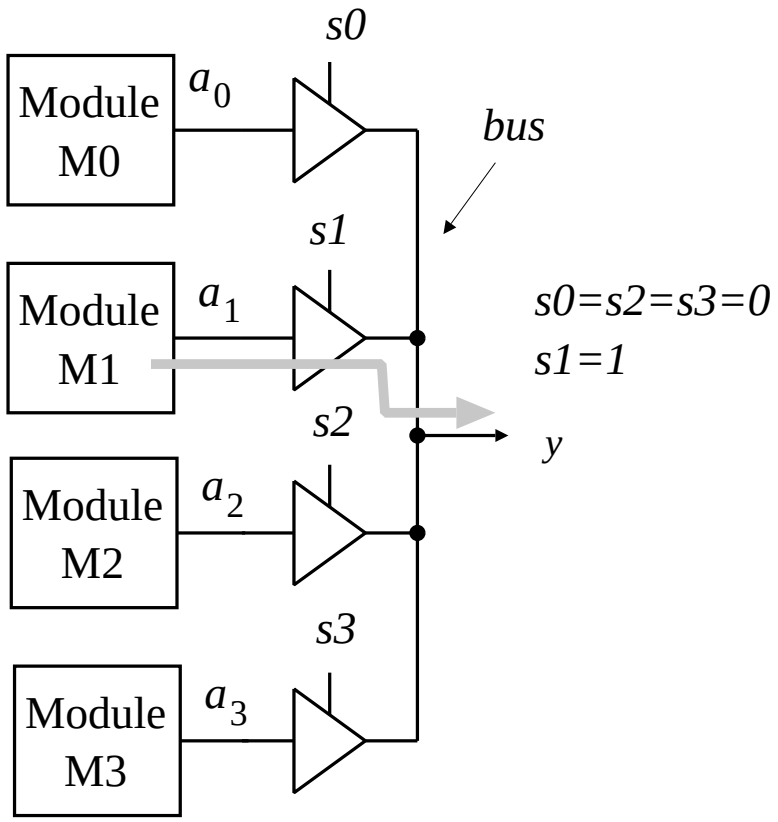


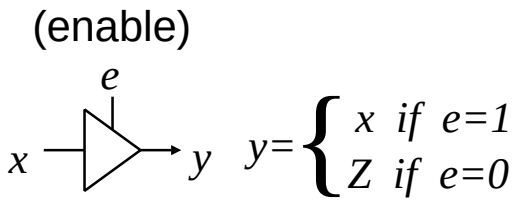
Figure 3.15: GATE NETWORK FOR SELECTING A MODULE OUTPUT.

THREE-STATE DRIVER (BUFFER)

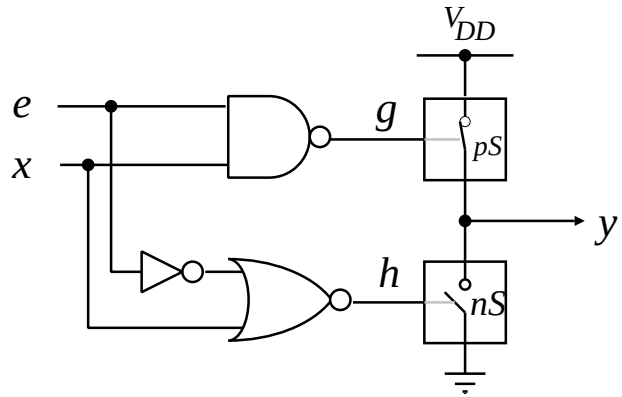


(c)

Figure 3.16: c) EXAMPLE OF USE OF THREE-STATE DRIVERS



(a)



e	x	g	h	pS	nS	y
0	0	1	0	open	open	Z
0	1	1	0	open	open	Z
1	0	1	1	open	closed	0
1	1	0	0	closed	open	1

three-state circuit

three-state circuit operation

(b)

Figure 3.16: a) THREE-STATE GATE: SYMBOL AND FUNCTION. b) CIRCUIT AND OPERATION.

Table 3.2: Characteristics of a family of CMOS gates

Gate type	Fan-in	Propagation delays		Load factor	Size
		t_{pLH} [ns]	t_{pHL} [ns]	[standard loads]	[equiv. gates]
AND	2	$0.15 + 0.037L$	$0.16 + 0.017L$	1.0	2
AND	3	$0.20 + 0.038L$	$0.18 + 0.018L$	1.0	2
AND	4	$0.28 + 0.039L$	$0.21 + 0.019L$	1.0	3
OR	2	$0.12 + 0.037L$	$0.20 + 0.019L$	1.0	2
OR	3	$0.12 + 0.038L$	$0.34 + 0.022L$	1.0	2
OR	4	$0.13 + 0.038L$	$0.45 + 0.025L$	1.0	3
NOT	1	$0.02 + 0.038L$	$0.05 + 0.017L$	1.0	1
NAND	2	$0.05 + 0.038L$	$0.08 + 0.027L$	1.0	1
NAND	3	$0.07 + 0.038L$	$0.09 + 0.039L$	1.0	2
NAND	4	$0.10 + 0.037L$	$0.12 + 0.051L$	1.0	2
NAND	5	$0.21 + 0.038L$	$0.34 + 0.019L$	1.0	4
NAND	6	$0.24 + 0.037L$	$0.36 + 0.019L$	1.0	5
NAND	8	$0.24 + 0.038L$	$0.42 + 0.019L$	1.0	6
NOR	2	$0.06 + 0.075L$	$0.07 + 0.016L$	1.0	1
NOR	3	$0.16 + 0.111L$	$0.08 + 0.017L$	1.0	2
NOR	4	$0.23 + 0.149L$	$0.08 + 0.017L$	1.0	4
NOR	5	$0.38 + 0.038L$	$0.23 + 0.018L$	1.0	4
NOR	6	$0.46 + 0.037L$	$0.24 + 0.018L$	1.0	5
NOR	8	$0.54 + 0.038L$	$0.23 + 0.018L$	1.0	6
XOR	2*	$0.30 + 0.036L$	$0.30 + 0.021L$	1.1	3
		$0.16 + 0.036L$	$0.15 + 0.020L$	2.0	
XOR	3*	$0.50 + 0.038L$	$0.49 + 0.027L$	1.1	6
		$0.28 + 0.039L$	$0.27 + 0.027L$	2.4	
		$0.19 + 0.036L$	$0.17 + 0.025L$	2.1	
XNOR	2*	$0.30 + 0.036L$	$0.30 + 0.021L$	1.1	3
		$0.16 + 0.036L$	$0.15 + 0.020L$	2.0	
XNOR	3*	$0.50 + 0.038L$	$0.49 + 0.027L$	1.1	6
		$0.28 + 0.039L$	$0.27 + 0.027L$	2.3	
		$0.19 + 0.036L$	$0.17 + 0.025L$	1.3	
2-OR/NAND2	4	$0.17 + 0.075L$	$0.10 + 0.028L$	1.0	2
2-AND/NOR2	4	$0.17 + 0.075L$	$0.10 + 0.028L$	1.0	2

LEVELS OF INTEGRATION

Level of Integration	Technology	Number of transistors	Typical functions
SSI	bipolar	≈ 10	Individual gates, flip-flops
MSI	MOS, bipolar	10-100	Adders, counters, registers
LSI	MOS, bipolar	100-10,000	ROMs, PLAs, small memories
VLSI	MOS, bipolar	$> 10{,}000$	large memories, microprocessors, complex systems

FULL-CUSTOM
SEMI-CUSTOM (standard cells)
GATE-ARRAY

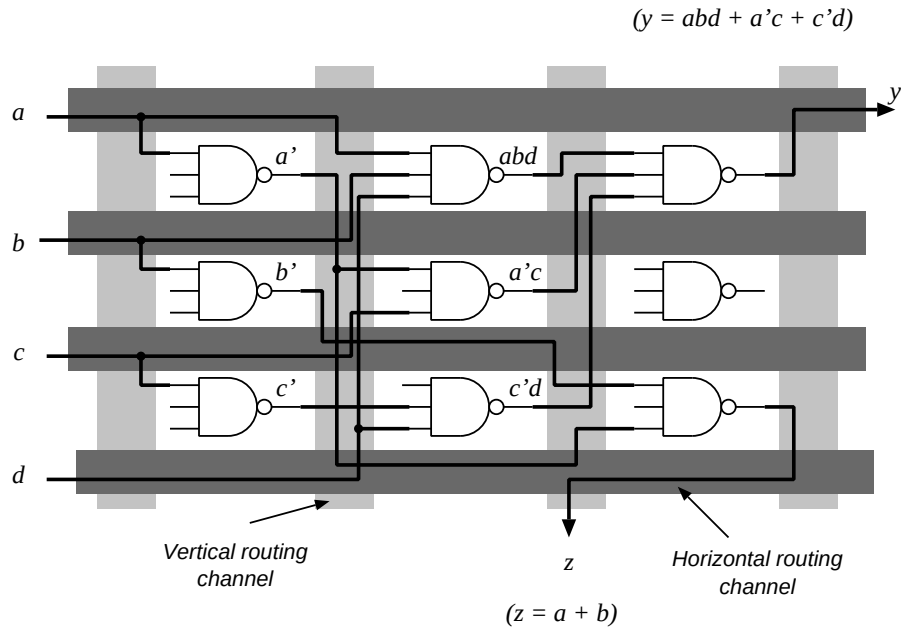


Figure 3.17: EXAMPLE OF GATE ARRAY.

PACKAGING LEVEL: CHIPS, BOARDS, AND CABINETS

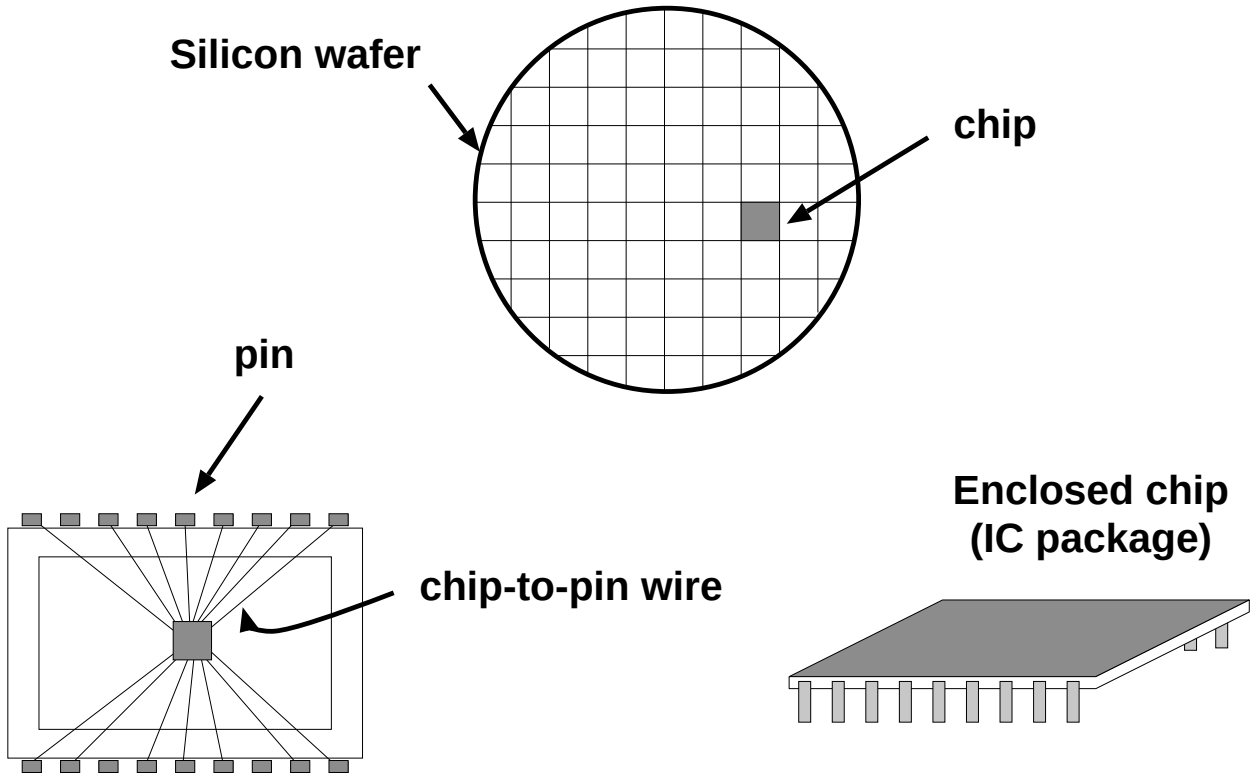


Figure 3.18: SILICON WAFER, CHIP AND INTEGRATED CIRCUIT PACKAGE

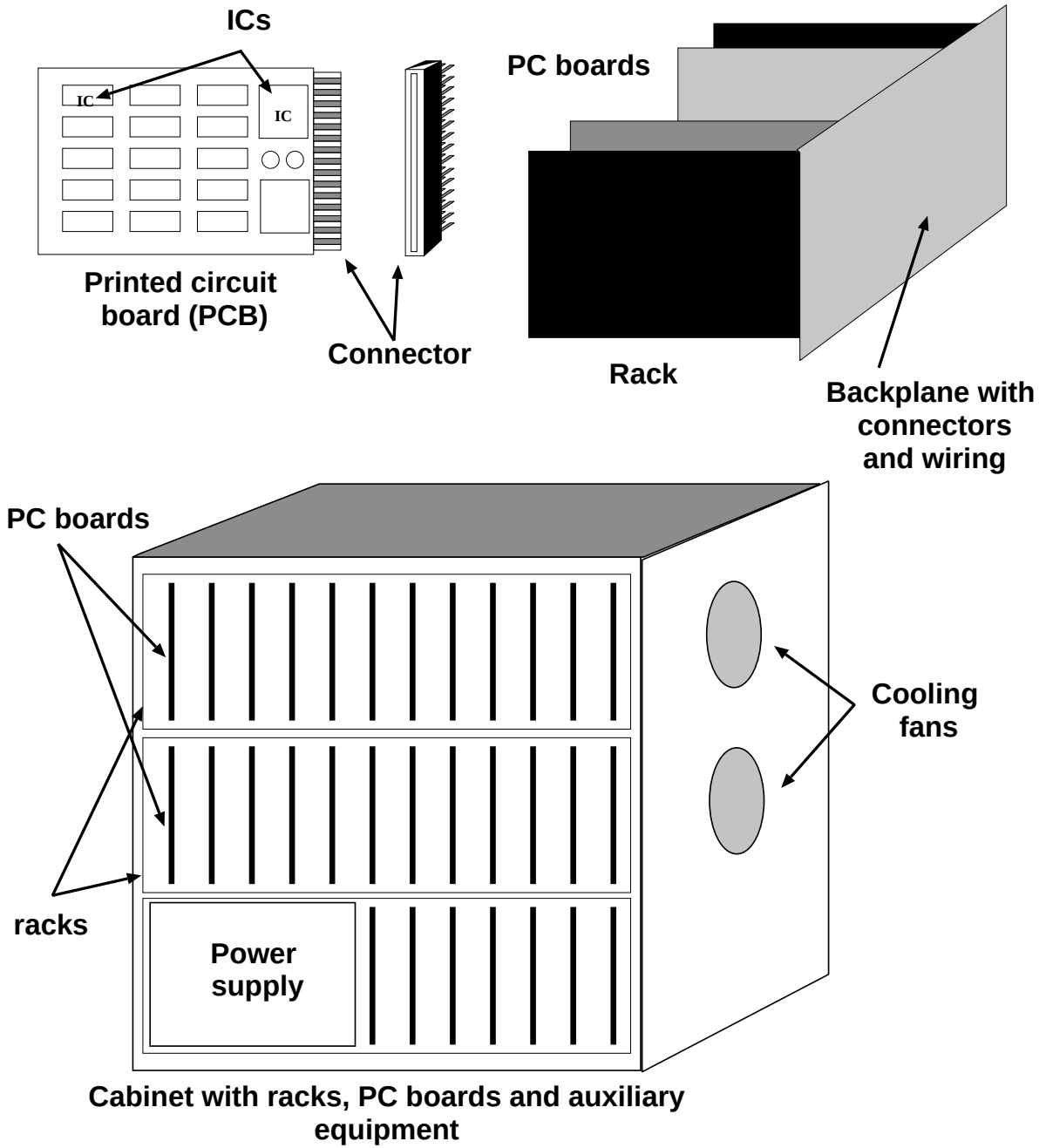


Figure 3.19: PACKAGING LEVELS

PACKAGING LEVELS: EXAMPLE

IBM 3081 central processing unit:

Level of Packaging	Number of Components	Size [mm×mm]
Module	100–133 chips	90×90
PC Board	6 – 9 modules	600×700
Subsystem (processor)	3 boards	
System (CPU)	2 subsystems	