DESCRIPTION AND ANALYSIS OF GATE NETWORKS

- GATE NETWORKS
- SETS OF GATES: (AND OR NOT), NAND NOR XOR
- ANALYSIS AND DESCRIPTION OF GATE NETWORKS

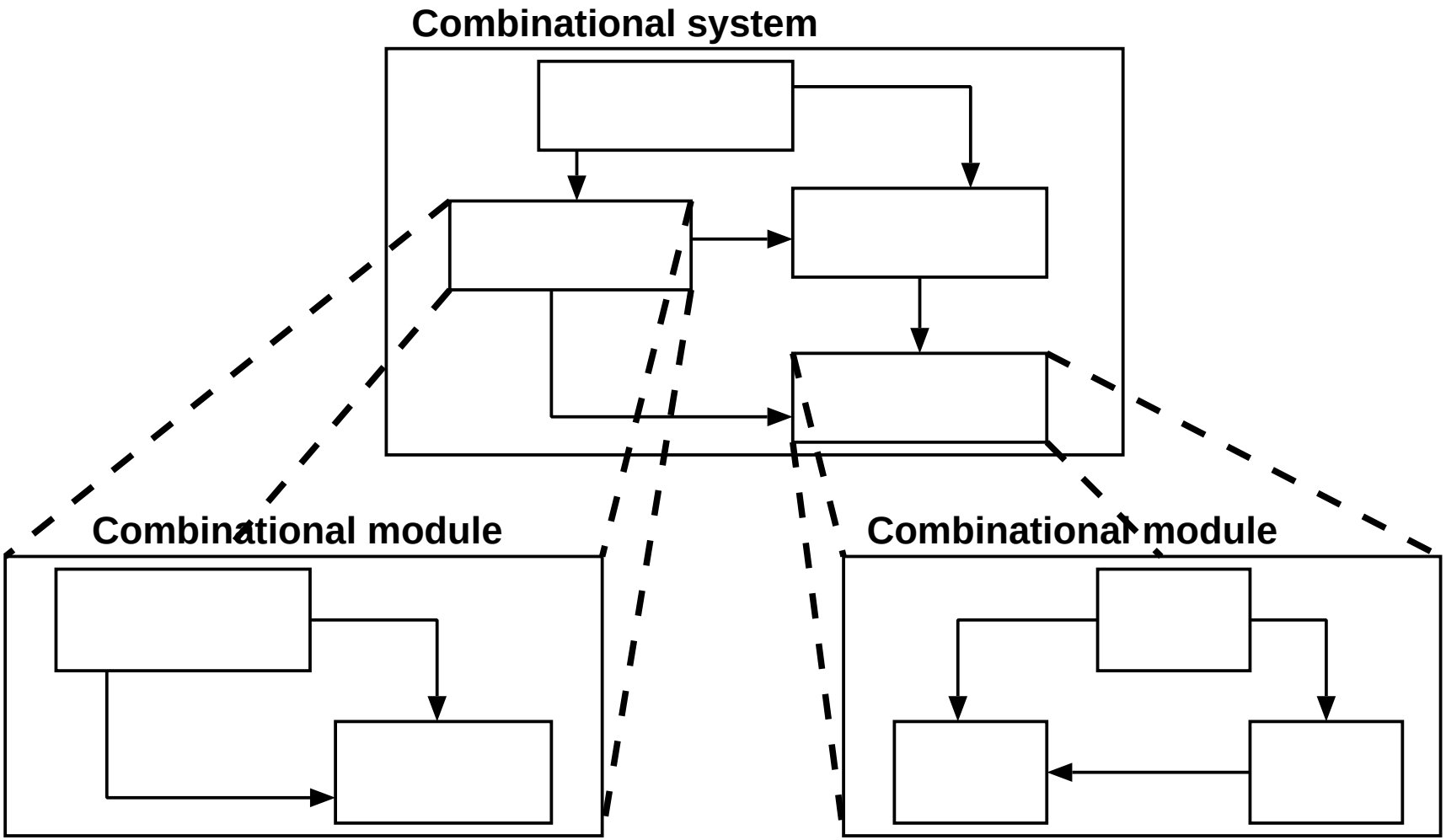


Figure 4.1: HIERARCHICAL IMPLEMENTATION OF A MODULE

GATE NETWORKS

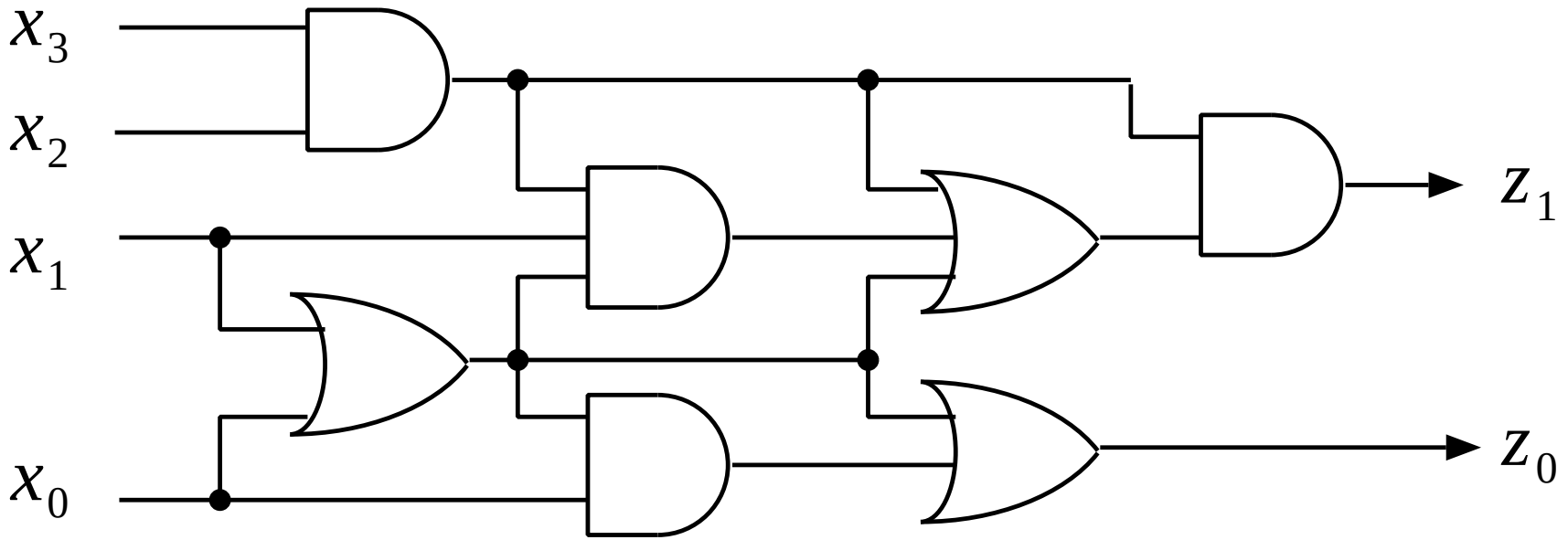


Figure 4.2: A GATE NETWORK

- GATES
- EXTERNAL INPUTS AND OUTPUTS
- CONNECTIONS

GATE NETWORKS (cont.)

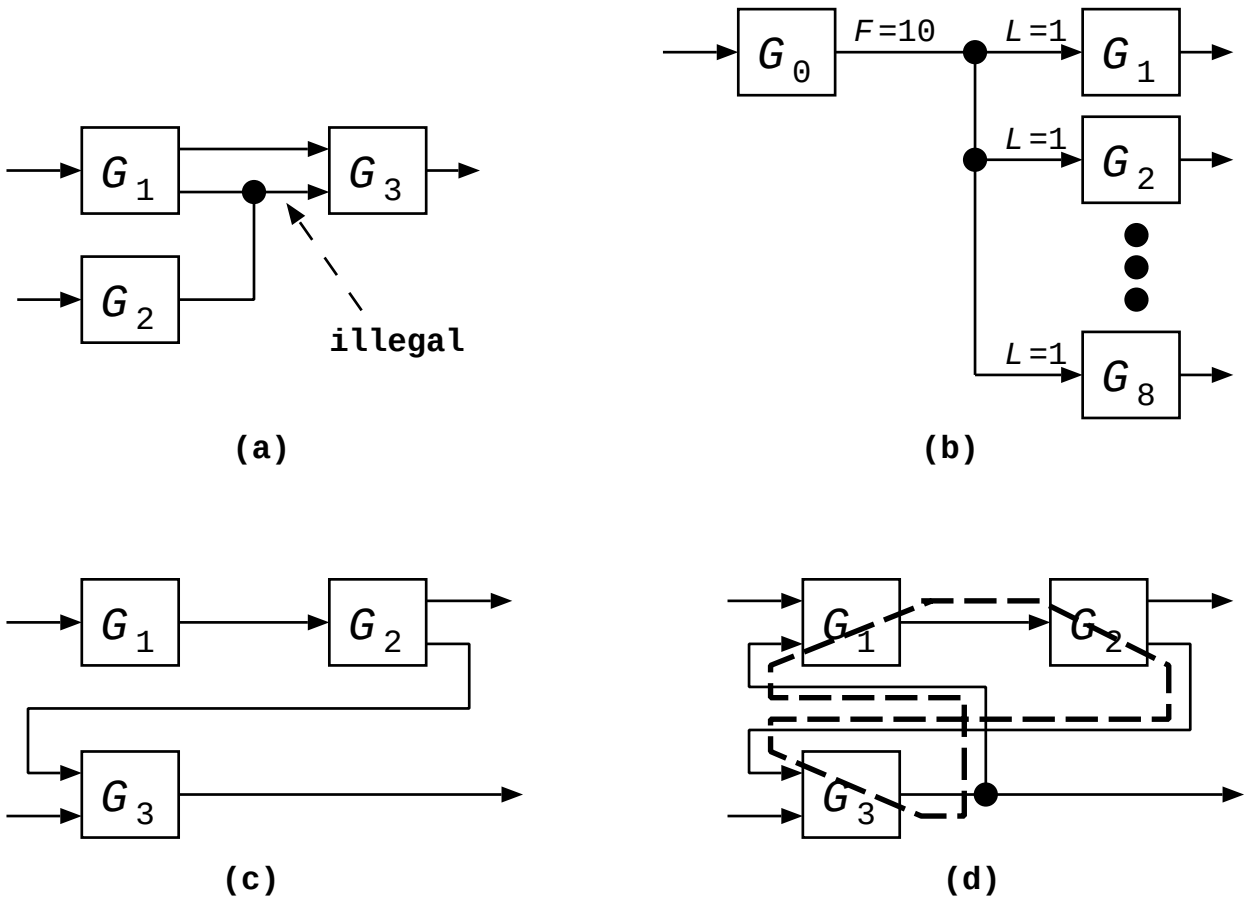


Figure 4.3: a) ILLEGAL NETWORK CONNECTION. b) ACCEPTABLE OUTPUT LOAD. c) LOOP-FREE NETWORK. d) LOOP NETWORK

DESCRIPTION OF GATE NETWORKS

- LOGIC DIAGRAM (GRAPHICAL REPRESENTATION)
- NET LIST (TABULAR REPRESENTATION)
- HDL DESCRIPTION (PROGRAM)

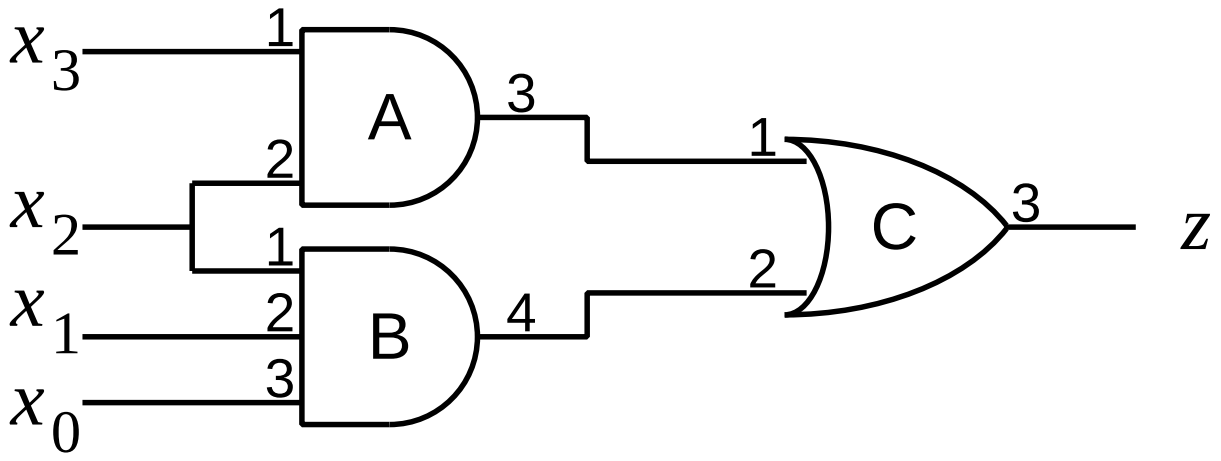


Figure 4.4: a) GRAPHICAL REPRESENTATION (LOGIC DIAGRAM)

Gate	Type	Inputs	Output
A	$\text{AND} - 2$	A_1	A_3
		A_2	
B	$\text{AND} - 3$	B_1	B_4
		B_2	
		B_3	
C	$\text{OR} - 2$	C_1	C_3
		C_2	

Gates

From	To
x_3	A_1
x_2	A_2
x_2	B_1
x_1	B_2
x_0	B_3
A_3	C_1
B_4	C_2
C_3	z

Connections

(b)

```
A_3 <= x3 and x2;
B_4 <= x2 and x1 and x0;
C_3 <= A_3 or B_4;
z   <= C_3;
```

(c)

Figure 4.4: NETWORK REPRESENTATION: a) GRAPHICAL; b) TABULAR; c) HDL-BASED.

CHARACTERIZATION OF A GATE NETWORK

- FUNCTIONAL SPECIFICATION
- INPUT LOAD FACTORS OF THE NETWORK INPUTS;
- FAN-OUT FACTOR OF THE NETWORK OUTPUTS (ONLY FOR SOME TECHNOLOGIES); AND
- PROPAGATION DELAYS THROUGH THE NETWORK

UNIVERSAL SETS OF GATES

- Set {AND,OR,NOT}

$$z = (((x_0 + x_1)x_2)' + x_2x_3 + x_4)'$$

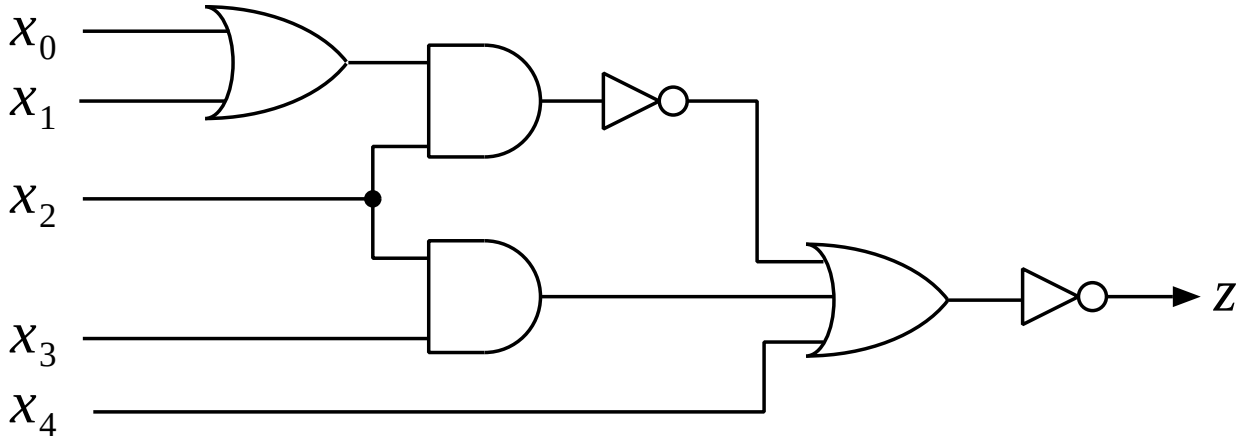


Figure 4.5: CORRESPONDENCE AMONG SWITCHING EXPRESSION ANd AND-OR-NOT NETWORK

UNIVERSAL SETS OF GATES (cont.)

- Sets {AND,NOT} and {OR,NOT}

$$x_{n-1} + x_{n-2} + \ldots x_i + \ldots x_0 = (x'_{n-1}x'_{n-2}\ldots x'_i \ldots x'_0)'$$

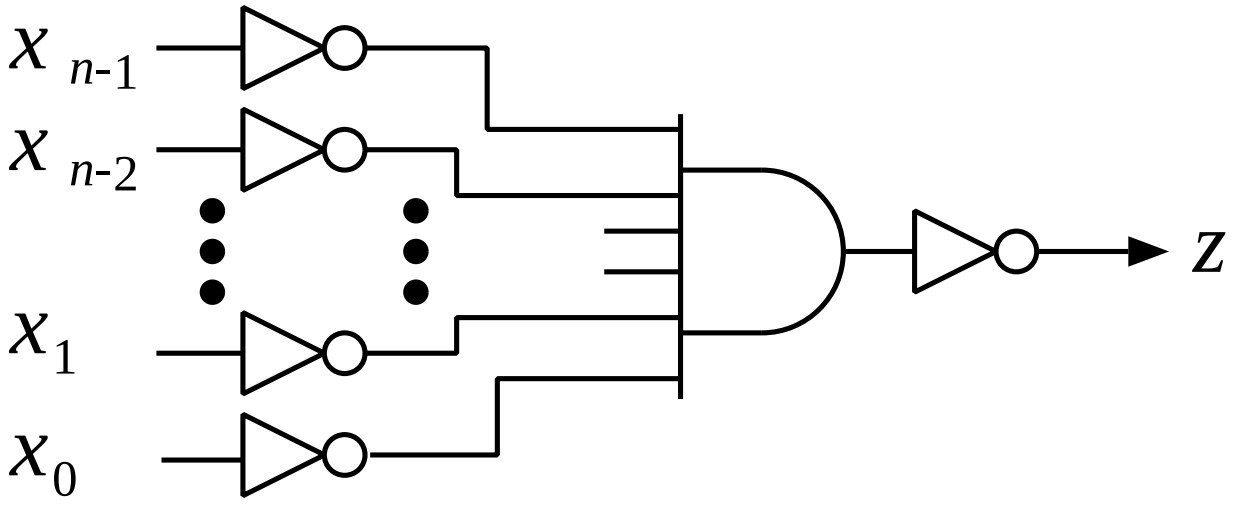


Figure 4.6: AND-NOT IMPLEMENTATION OF AN OR GATE

UNIVERSAL SETS OF GATES (cont.)

- Sets {NAND} and {NOR}

$$x' = (xx)'$$

$$NOT(x) = NAND(x, x)$$

$$x_1x_0 = ((x_1x_0)')' = ((x_1x_0)'(x_1x_0)')'$$

$$AND(x_1, x_0) = NAND(NAND(x_1, x_0), NAND(x_1, x_0))$$

UNIVERSAL SETS OF GATES (cont.)

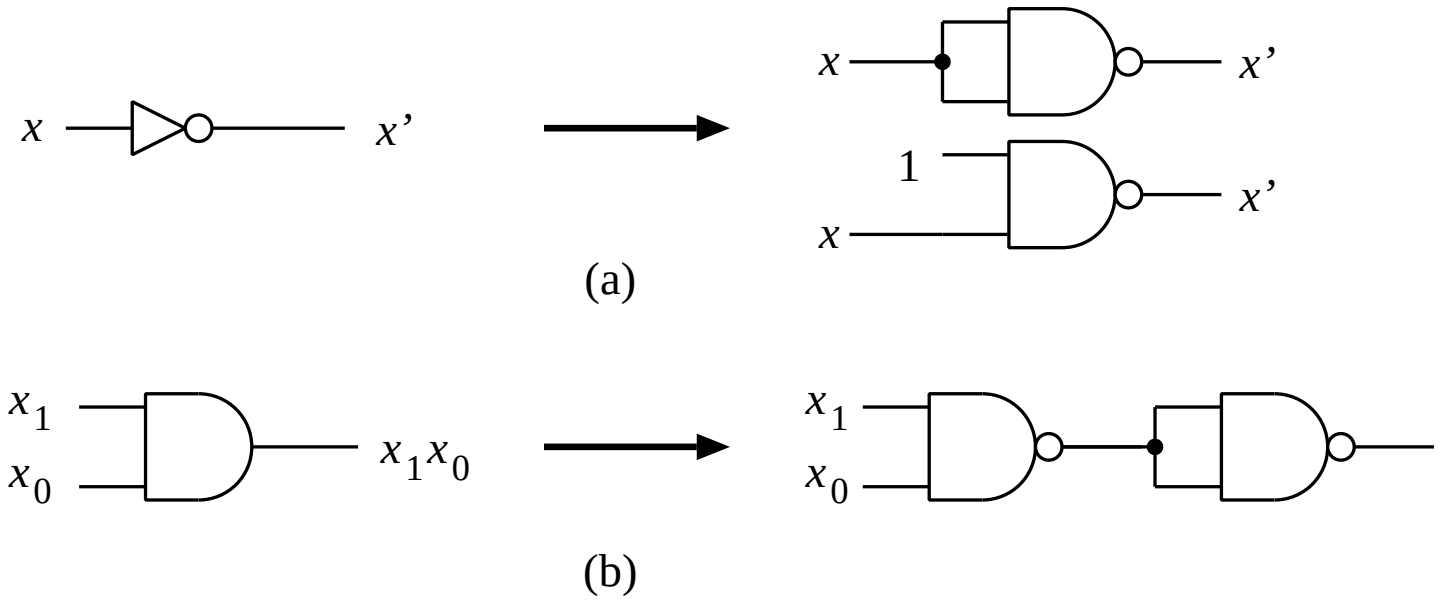


Figure 4.7: IMPLEMENTATIONS WITH NAND GATES: a) NOT; b) AND

MIXED-LOGIC NOTATION

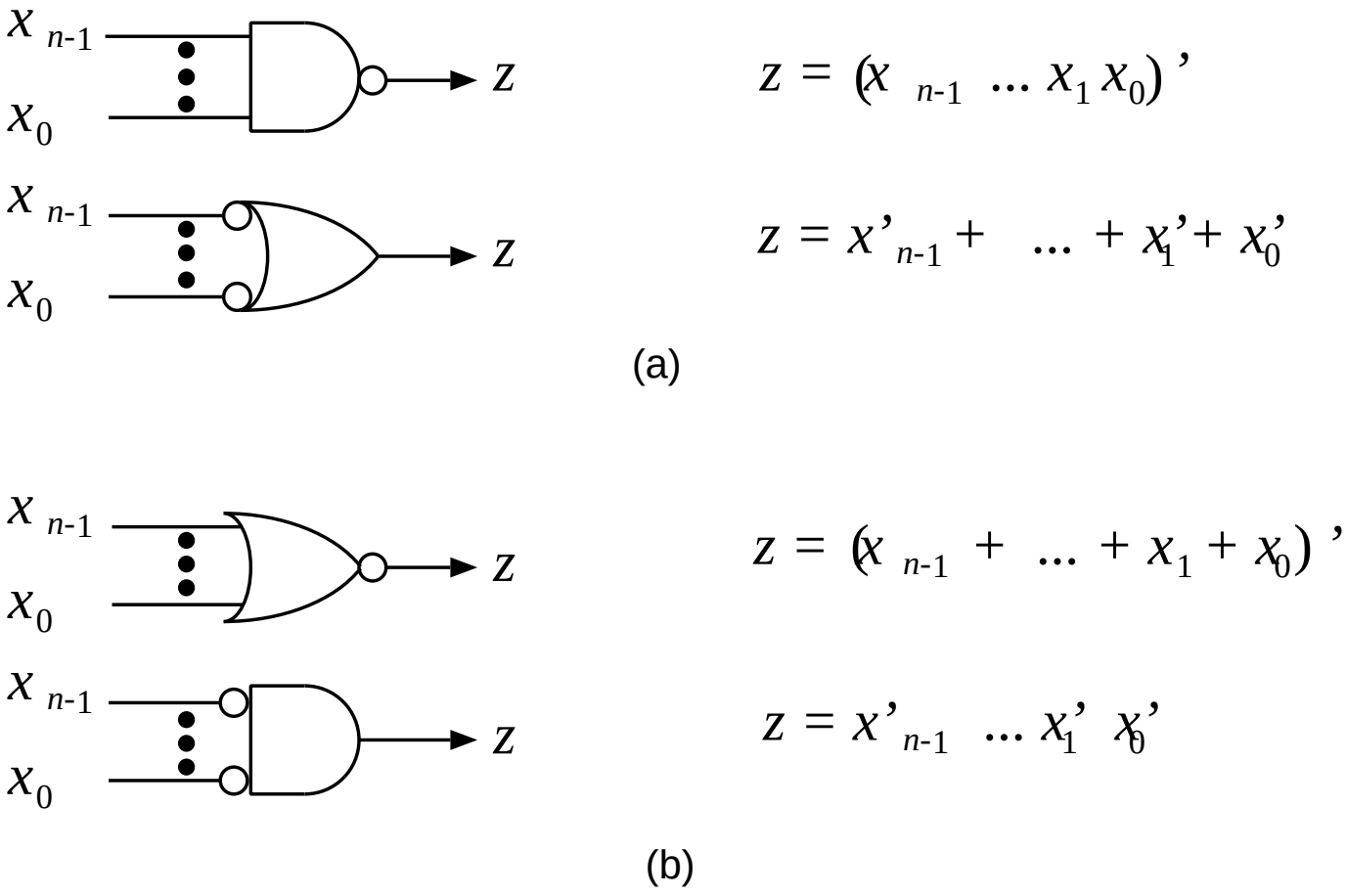


Figure 4.8: MIXED-LOGIC NOTATION: a) NAND GATE b) NOR GATE

COMPLEX GATE STRUCTURES

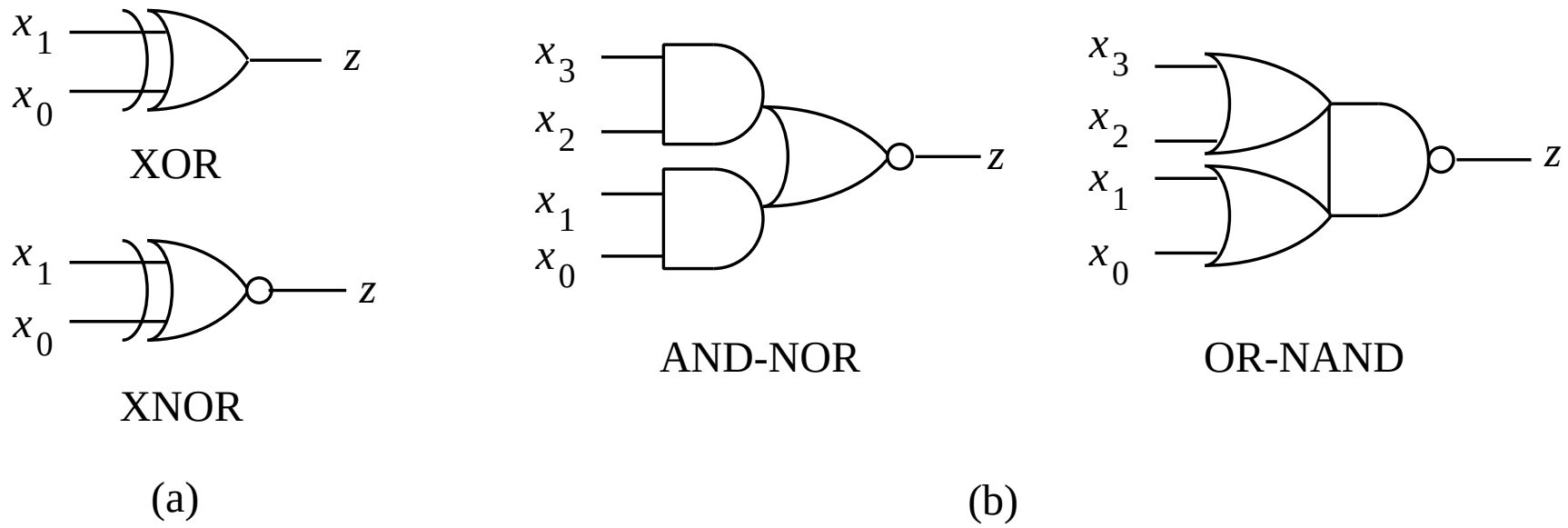


Figure 4.9: ADDITIONAL GATES IN CMOS a) XOR and XNOR, b) COMPLEX GATE STRUCTURES: AND-OR and OR-AND

ANALYSIS OF GATE NETWORKS

- FUNCTIONAL ANALYSIS:
  1. OBTAIN I/O SWITCHING EXPRESSIONS
  2. OBTAIN A TABULAR REPRESENTATION OF THE (BINARY) FUNCTION (IF FEW VARIABLES)
  3. DEFINE HIGH-LEVEL INPUT AND OUTPUT VARIABLES;
     USE CODES TO RELATE THESE VARIABLES WITH THE BIT-VECTORS
  4. OBTAIN A HIGH-LEVEL SPECIFICATION OF THE SYSTEM

- NETWORK CHARACTERISTICS:
  INPUT LOAD FACTORS, FAN-OUT FACTORS, AND DELAYS

OBTAIN SWITCHING EXPRESSIONS

- ASSIGN NAMES TO EACH CONNECTION IN THE NETWORK
- WRITE SWITCHING EXPRESSIONS FOR EACH GATE OUTPUT
- SUBSTITUTE ALL INTERNAL NAMES TO OBTAIN EXTERNAL OUTPUTS IN TERMS OF EXTERNAL INPUTS

Example

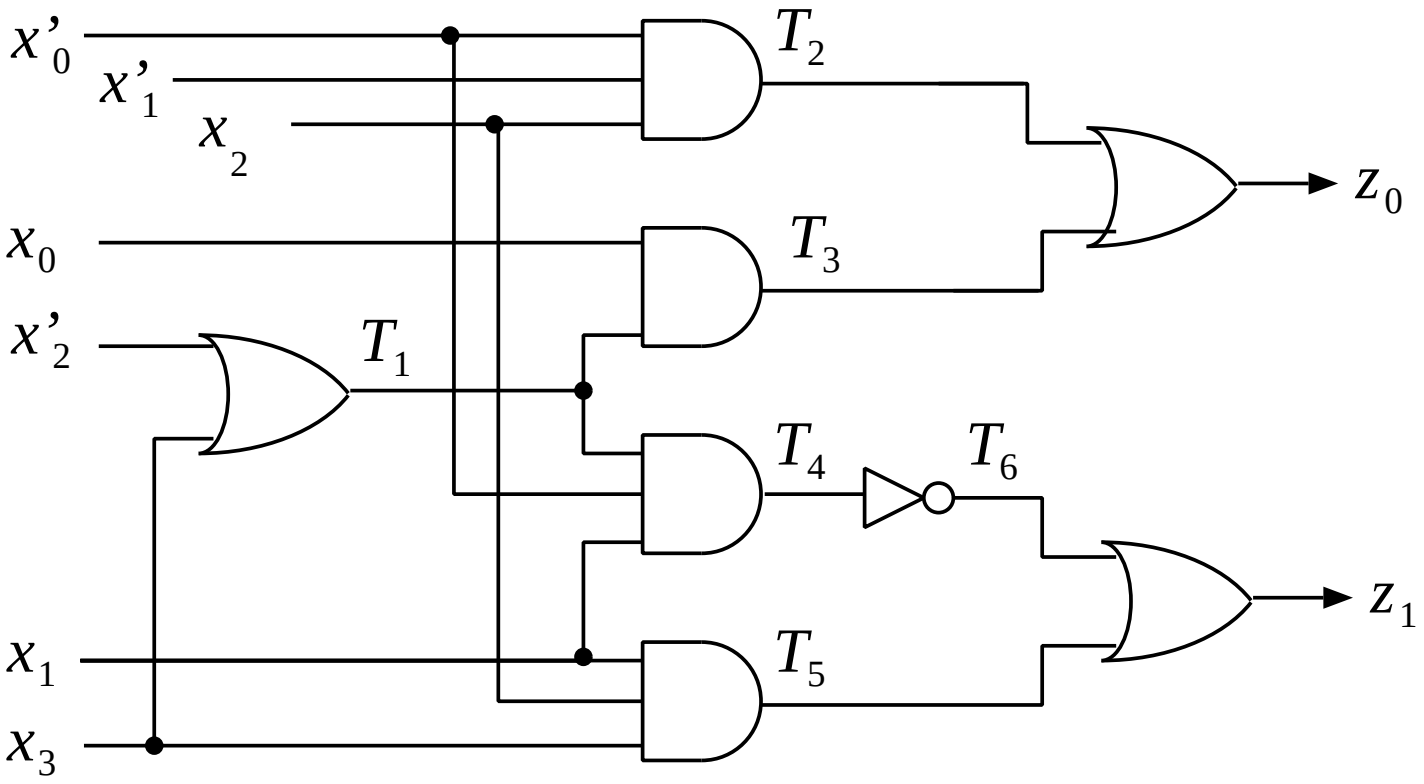


Figure 4.10: GATE NETWORK FOR ANALYSIS

EXAMPLE (cont.)

OUTPUT EXPRESSIONS:

$$\begin{aligned} z_0 &= T_2 + T_3 \\ &= x_0' x_1' x_2 + x_0 T_1 \\ &= x_0' x_1' x_2 + x_0 (x_2' + x_3) \\ &= x_0' x_1' x_2 + x_0 x_2' + x_0 x_3 \end{aligned}$$

$$\begin{aligned} z_1 &= T_5 + T_6 \\ &= x_1 x_2 x_3 + T_4' \\ &= x_1 x_2 x_3 + (T_1 x_0' x_1)' \\ &= x_1 x_2 x_3 + T_1' + x_0 + x_1' \\ &= x_1 x_2 x_3 + x_2 x_3' + x_0 + x_1' \end{aligned}$$

REDUCED EXPRESSIONS:

$$\begin{aligned} z_0 &= x_0' x_1' x_2 + x_0 x_2' + x_0 x_3 \quad \text{(no reduction possible)} \\ z_1 &= x_0 + x_1' + x_2 \end{aligned}$$

HIERARCHICAL APPROACH

- DECOMPOSE THE NETWORK INTO SUBNETWORKS (MODULES)
- ANALYZE EACH SUBNETWORK SEPARATELY
- USE SUBSTITUTION TO OBTAIN THE NETWORK FUNCTION

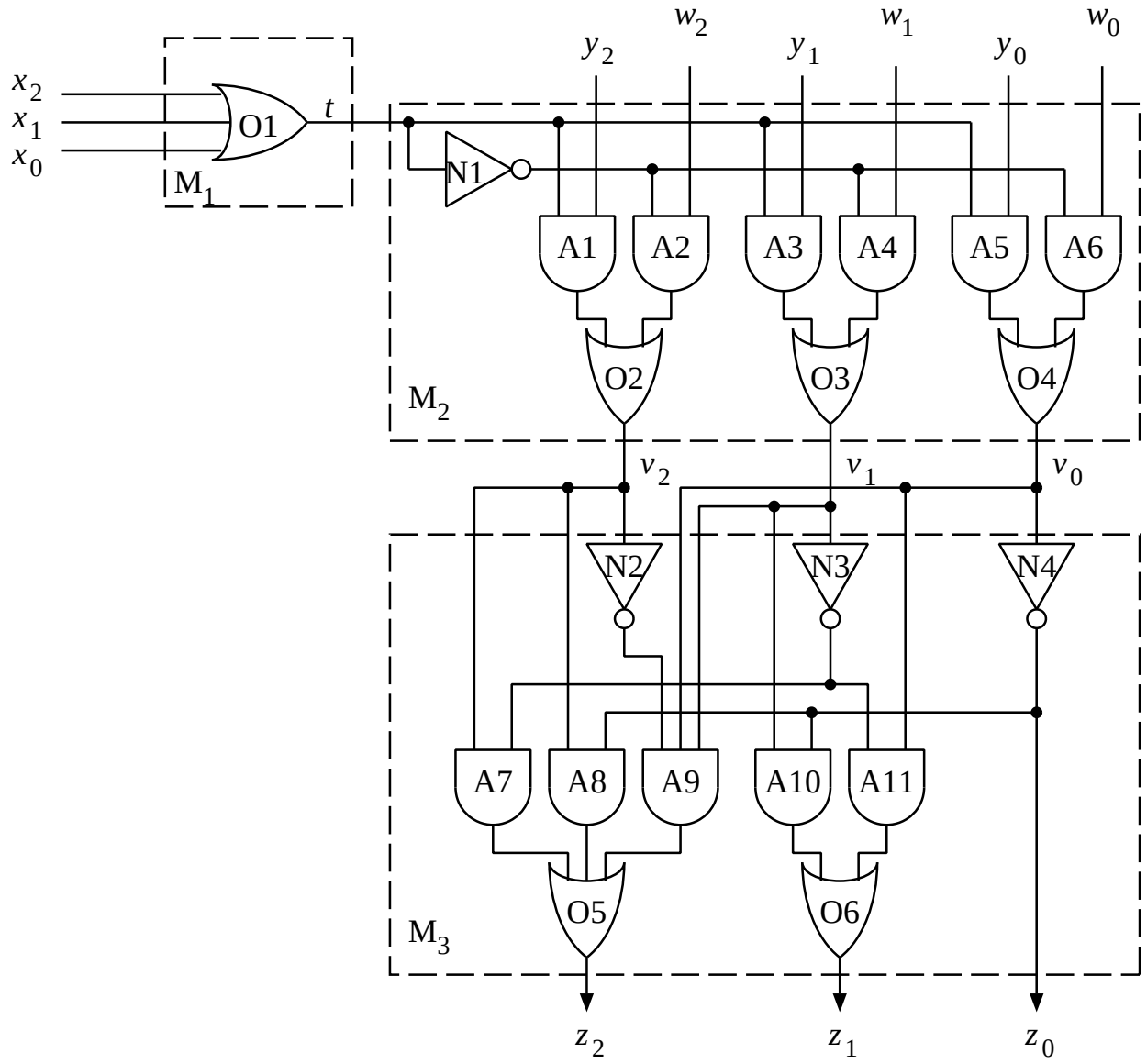


Figure 4.11: NETWORK FOR HIERARCHICAL ANALYSIS

EXAMPLE cont.

VERIFY THAT THE NETWORK SATISFIES THE SPECIFICATION:

Inputs: $x, y, w \in \{0, 1, \ldots, 7\}$

Output: $z \in \{0, 1, \ldots, 7\}$

Function: $$z = \begin{cases} (y+1) \bmod 8 & \textbf{if} \quad x \neq 0 \\ (w+1) \bmod 8 & \textbf{if} \quad x = 0 \end{cases}$$

- SUBNETWORKS

M_1:

$$t = x_2 + x_1 + x_0$$

$$t = \begin{cases} 1 & \textbf{if} \quad x \neq 0 \\ 0 & \textbf{otherwise} \end{cases}$$

M_2:

$$v_i = y_i t + w_i t' \quad (i = 0, 1, 2)$$

$$\underline{v} = \begin{cases} \underline{y} & \textbf{if} \quad t = 1 \\ \underline{w} & \textbf{if} \quad t = 0 \end{cases}$$

$$v = \begin{cases} y & \textbf{if} \quad t = 1 \\ w & \textbf{if} \quad t = 0 \end{cases}$$

M_3:

$$\begin{aligned} z_2 &= v_2' v_1 v_0 + v_2 v_1' + v_2 v_0' \\ z_1 &= v_1 v_0' + v_1' v_0 \\ z_0 &= v_0' \end{aligned}$$

EXAMPLE (cont.)

- HIGH-LEVEL SPECIFICATION:

v_2	v_1	v_0	z_2	z_1	z_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

$\rightarrow$

v	z
0	1
1	2
2	3
3	4
4	5
5	6
6	7
7	0

FROM TABLE, WE GET

$$z = (v + 1) \bmod 8$$

SECOND LEVEL OF ANALYSIS:

$$z = \begin{cases} (y + 1) \bmod 8 & \textbf{if} \quad x \neq 0 \\ (w + 1) \bmod 8 & \textbf{if} \quad x = 0 \end{cases}$$

ANALYSIS OF NETWORKS WITH NOT, NAND and NOR

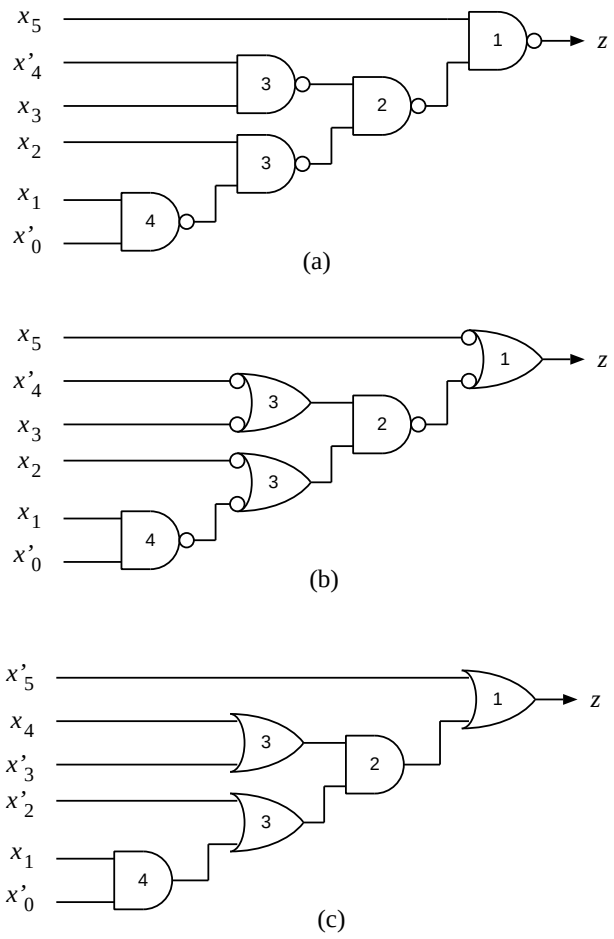
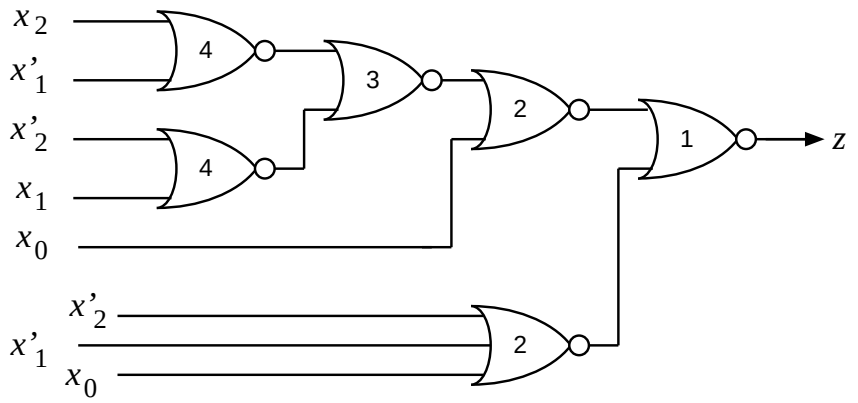


Figure 4.12: a) NAND NETWORK; b) NETWORK REDRAWN IN MIXED-LOGIC NOTATION

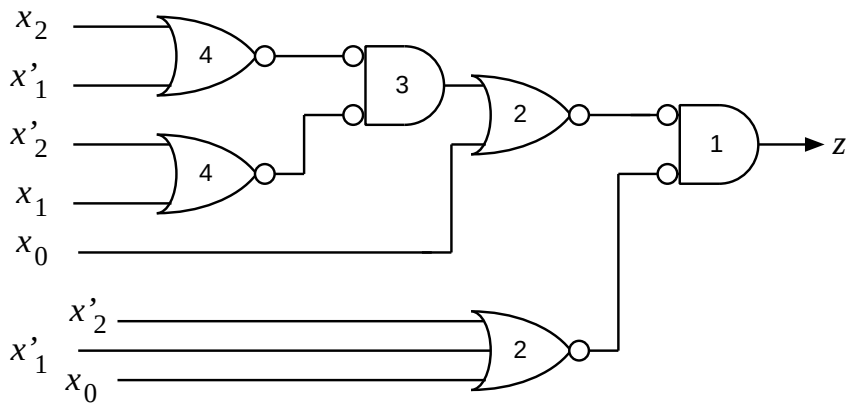
ANALYSIS (cont.)

- USE MIXED-LOGIC TRANSFORMATIONS

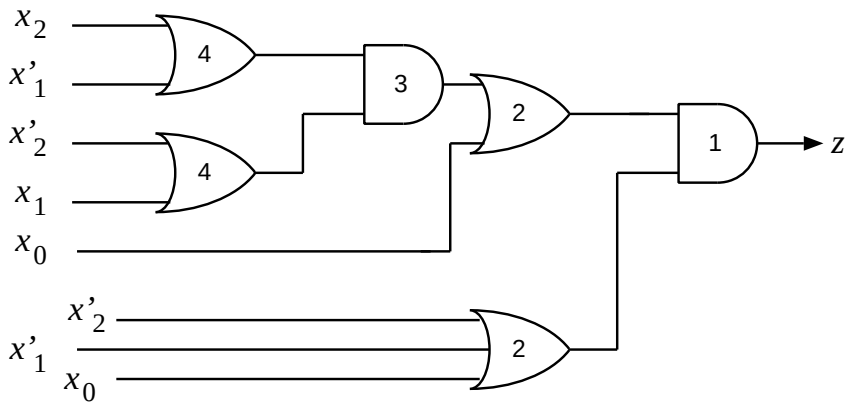
$$
\begin{aligned}
z &= x_5' + (x_4 + x_3')(x_2' + x_1 x_0') \\
&= x_5' + x_4 x_2' + x_3 x_2' + x_4 x_1 x_0' + x_3' x_1 x_0'
\end{aligned}
$$



(a)



(b)



(c)

Figure 4.13: a) NOR NETWORK; b) NETWORK REDRAWN IN MIXED-LOGIC NOTATION

ANALYSIS (cont.)

$$
\begin{aligned}
z &= ((x_2 + x_1')(x_2' + x_1) + x_0)(x_2' + x_1' + x_0') \\
&= (x_2 + x_1' + x_0)(x_2' + x_1 + x_0)(x_2' + x_1' + x_0') \\
&= (x_2 x_1 + x_2' x_1' + x_0)(x_2' + x_1' + x_0) \\
&= x_2' x_1' + x_0
\end{aligned}
$$

ANALYSIS OF CHARACTERISTICS

- LOAD FACTOR OF A NETWORK INPUT
- FAN-OUT FACTOR OF A NETWORK OUTPUT
- SIZE OF THE NETWORK
- NETWORK (PROPAGATION) DELAY
- NUMBER OF LEVELS OF A NETWORK
- DYNAMIC CHARACTERISTICS

Table 4.3: Characteristics of a family of CMOS gates

Gate type	Fan-in	Propagation delays		Load factor	Size
		t_{pLH} [ns]	t_{pHL} [ns]	[standard loads]	[equiv. gates]
AND	2	$0.15 + 0.037L$	$0.16 + 0.017L$	1.0	2
AND	3	$0.20 + 0.038L$	$0.18 + 0.018L$	1.0	2
AND	4	$0.28 + 0.039L$	$0.21 + 0.019L$	1.0	3
OR	2	$0.12 + 0.037L$	$0.20 + 0.019L$	1.0	2
OR	3	$0.12 + 0.038L$	$0.34 + 0.022L$	1.0	2
OR	4	$0.13 + 0.038L$	$0.45 + 0.025L$	1.0	3
NOT	1	$0.02 + 0.038L$	$0.05 + 0.017L$	1.0	1
NAND	2	$0.05 + 0.038L$	$0.08 + 0.027L$	1.0	1
NAND	3	$0.07 + 0.038L$	$0.09 + 0.039L$	1.0	2
NAND	4	$0.10 + 0.037L$	$0.12 + 0.051L$	1.0	2
NAND	5	$0.21 + 0.038L$	$0.34 + 0.019L$	1.0	4
NAND	6	$0.24 + 0.037L$	$0.36 + 0.019L$	1.0	5
NAND	8	$0.24 + 0.038L$	$0.42 + 0.019L$	1.0	6
NOR	2	$0.06 + 0.075L$	$0.07 + 0.016L$	1.0	1
NOR	3	$0.16 + 0.111L$	$0.08 + 0.017L$	1.0	2
NOR	4	$0.23 + 0.149L$	$0.08 + 0.017L$	1.0	4
NOR	5	$0.38 + 0.038L$	$0.23 + 0.018L$	1.0	4
NOR	6	$0.46 + 0.037L$	$0.24 + 0.018L$	1.0	5
NOR	8	$0.54 + 0.038L$	$0.23 + 0.018L$	1.0	6
XOR	2*	$0.30 + 0.036L$	$0.30 + 0.021L$	1.1	3
		$0.16 + 0.036L$	$0.15 + 0.020L$	2.0	

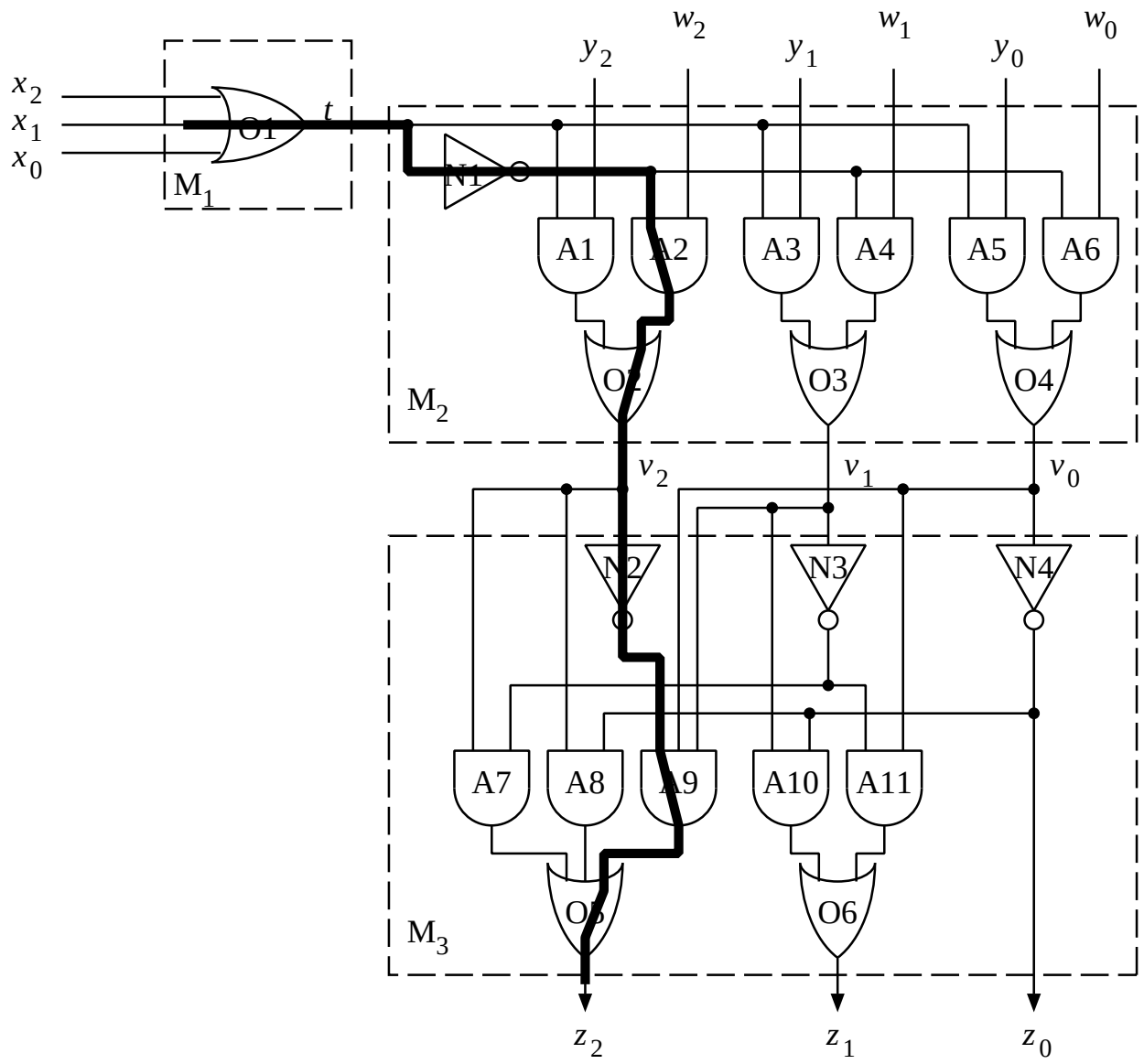


Figure 4.14: NETWORK FOR HIERARCHICAL ANALYSIS

EXAMPLE (cont.)

TYPES OF GATES USED: 2-input AND, 3-input AND, etc.

LOAD FACTORS: NETWORK INPUTS: 1; GATE INPUTS: 1

FANOUT FACTORS: $F = 12$ (assumed)

$$F(z_2) = F(z_1) = 12, \quad F(z_0) = 12 - 2 = 10$$

NETWORK SIZE : 38 [equiv. gates] 21 [actual]

NUMBER OF LEVELS: 7

NETWORK DELAY Example of path delay calculation:

$$O_1 \rightarrow N_1 \rightarrow A_2 \rightarrow O_2 \rightarrow N_2 \rightarrow A_9 \rightarrow O_5$$

$$\begin{aligned} T_{pLH}(x_1, z_2) &= t_{pLH}(O_1) + t_{pHL}(N_1) + t_{pHL}(A_2) + t_{pHL}(O_2) \\ &\quad + t_{pLH}(N_2) + t_{pLH}(A_9) + t_{pLH}(O_5) \\ T_{pHL}(x_1, z_2) &= t_{pHL}(O_1) + t_{pLH}(N_1) + t_{pLH}(A_2) + t_{pLH}(O_2) \\ &\quad + t_{pHL}(N_2) + t_{pHL}(A_9) + t_{pHL}(O_5) \end{aligned}$$

Gate	Identifier	Output load	t_{pLH} [ns]	t_{pHL} [ns]
OR3	O_1	4	0.27	0.43
NOT	N_1	3	0.13	0.10
AND2	A_2	1	0.19	0.18
OR2	O_2	3	0.23	0.26
NOT	N_2	1	0.06	0.07
AND3	A_9	1	0.24	0.20
OR3	O_5	L	$0.12 + 0.038L$	$0.34 + 0.022L$

$$\begin{aligned} T_{pLH}(x_1, z_2) &= 0.27 + 0.10 + 0.18 + 0.26 + 0.06 \\ &\quad + 0.24 + 0.12 + 0.038L = 1.23 + 0.038L \text{ [ns]} \\ T_{pHL}(x_1, z_2) &= 0.43 + 0.13 + 0.19 + 0.23 + 0.07 \\ &\quad + 0.20 + 0.34 + 0.022L = 1.59 + 0.022L \text{ [ns]} \end{aligned}$$

TIMING DIAGRAM

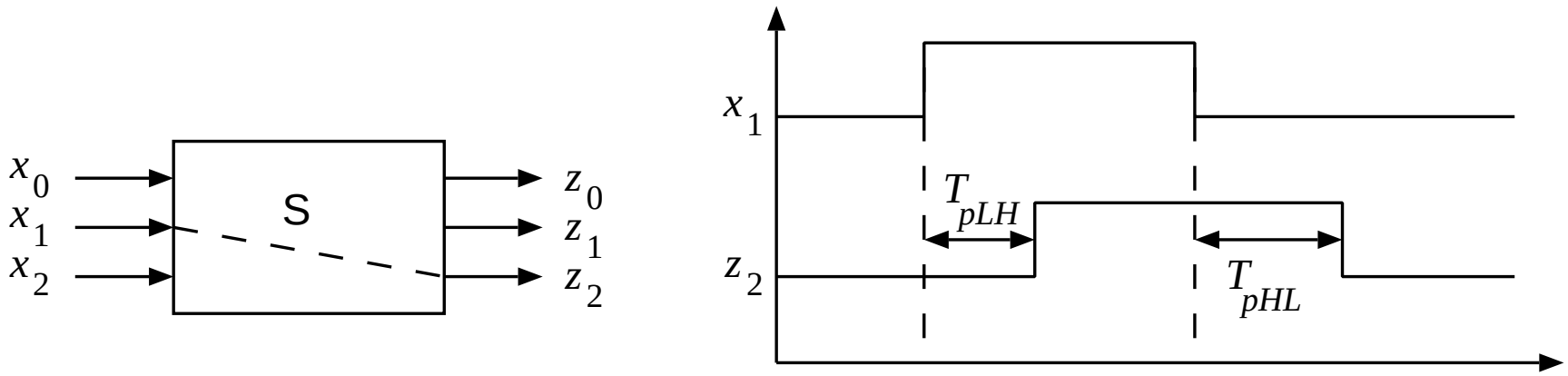


Figure 4.15: TIMING DIAGRAM FROM NETWORK ANALYSIS