LTEST 1.0

July 1992

Abstract

Many faculty are using the Abramovici, Breuer and Friedman text, " Digital Systems Testing and Testable Design ", published by Computer Science Press (1990), in a class on testing. They have expressed an interest to supplement their course with software tools. At USC we have developed such a suite of tools, called **LTEST 1.0**. It includes a good value simulator, a fault simulator, a fault collapsing module and a D-algorithm based ATPG module for combinational logic. The software has been specifically designed to be easily understood, modified and enhanced. The algorithms follow those described in the text. The software can be run in many modes, such as one module at a time, single step, interactively or as a batch process. Students can use the software " as is " to study the operation of various algorithms, e.g. simulation of a latch using different delay models and values. Also, simple programming projects can be given, such as extend the simulator from a 3-valued system to a 5-valued system; or change the D-algorithm so that it does only single path sensitization. There are numerous interesting software enhancements that can be made by changing only a small part of the code. The system is written in C and runs on a SUN4 workstation .

The code was not developed to be efficient in terms of CPU time and hence should not be used on large circuits.

We would be happy to act as an intermediary for sharing problems, fixes and/or bugs. Please send interesting problems and their solutions, on-line, to Prof. Breuer (mb@poisson.usc.edu). They will be distributed to those people who have been given a copy of this software. Also, we will attempt to resolve program bugs as they are pointed out to us.

The following is the current documenatation on **LTEST 1.0** as of 7/8/92. Sections 1-6 discuss the design of the software modules. Section 7 consists of a user's manual. Appendix A gives the grammar for describing the inputs to this system.

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