Course material: Lecture viewgraphs and class notes; readings; solutions; sample exams will be posted on the CourseWeb.


Grading: Homeworaks 10%, quizzes 20%, midterm 30%, final 40%.

TAs: Dis 2A - Gurupavan Mazumdar; Dis 2B - Sonali Garg; Dis 2C - Arulsaravana Jeyaraj

- Homeworks must be turned in at the beginning of discussion sessions - no exceptions!
- LogiSim Design Tool: used in discussion sessions. LogiSim is an easy to use schematic editor and logic simulator; free download at LogiSim.

CS M51A Fall 2018: Syllabus and Schedule. (Tentative - check for updates)

Week 1


- Tuesday, 10/2. Combinational systems: Binary specification of inputs/outputs and functions. Central concept of functional description: switching function (SF). Incompletely specified SFs. Basis of hierarchical specification and design: Composition of SFs. Switching algebra, switching expressions (SEs, evaluation of SEs, equivalent SEs, and algebraic transformations of SEs. Standard forms for SEs: sum of products (SOP) and product of sums (POS). Readings: Chapter 2, Appendix A.

Week 2


- Physical level: CMOS transistor switches and gates: NOT, NAND/NOR, AND/OR, and XOR. Readings: Chapter 3.

- HW1 posted. Friday, 10/5: Discussions.


Week 3
**HW2 posted.** Friday, 10/12: Discussions; HW1 due.


**Week 4**

• Thursday, 10/18. NAND and NOR networks. Programmable logic arrays (PLAs) and Field Programmable Gate Arrays (FPGAs). **Readings:** Chapter 5 and Chapter 12 (Sec on FPGAs). Examples of designs. 
**HW3 posted.** Friday, 10/19: Discussions, Quiz 1; HW2 due.


**Week 5**

**Friday, 10/26: Discussions, HW3 due.**

• Tuesday, 10/30. **MIDTERM EXAM – in class –.**
The exam covers Chapters 2, 3, 4, 5, and 7. Closed books and notes. Four cheat sheets allowed. Tables and identities given if needed. 
**HW4 posted.**

**Week 6**

**Friday, 11/2, Quiz 2.**


**Week 7**

**HW5 posted.** Friday, 11/9, HW4 due.

Week 8

  - **Friday, 11/16:** Quiz 3.

- **Tuesday, 11/20.** Comparators, arithmetic-logic units (ALUs), and multipliers for positive integers. **Readings:** Chapter 10.

Week 9

- **Tuesday, 11/27.** Standard sequential modules and networks: registers, shift registers, and counters. Their specifications, implementations, implementation of larger modules, and uses. **Readings:** Chapter 11.
  - **HW6 posted - a final exam sample – do not turn in.**

- **Thursday, 11/29.** Register Transfer Level (RTL) of specification and design. RTL system organization: data subsystem (datapath) and control subsystem. Types of datapaths and control. An RTL language and its use for description. **Readings:** Notes on RTL.
  - **Friday, 11/30:** Discussion. **HW5 due.**

Week 10

- **Tuesday, 12/4.** Examples of RTL systems – Specifications and designs:
  1. First-In-First-Out (FIFO) Memory
  2. Serial-Parallel Two’s Complement Multiplier
  **Readings:** Notes on FIFO and multiplier.

- **Thursday, 12/6.** Leftover material, course review, and Q/A.
  - **Friday, 12/7:** Quiz 4. **Solutions to HW6 posted.**

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- **FINAL EXAM, December 11, 8:00am - 11:00am, in class.** The exam is comprehensive with emphasis on Chapters 7, 8, 9, 10, and 11. Closed textbook and notes. Four cheat sheets allowed. Tables provided if needed.