Curriculum Vitae

Miloš D. Ercegovac
UCLA Computer Science Department
4731-H Boelter Hall
University of California
Los Angeles, CA 90024

Phone 310/825-5414, Fax 310/825-2273, e-mail: milos@cs.ucla.edu
www.cs.ucla.edu/~milos
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Education: Ph.D. degree (1975) and M.S. degree (1972) in Computer Science, University of Illinois, Urbana-Champaign, Illinois; B.S. degree (1965) in Electrical Engineering, University of Belgrade, Belgrade, Serbia.

Ph.D. Dissertation: *A General Method for Evaluation of Functions and Computations in a Digital Computer* (U. of Illinois, DCS Technical Report No. 750, 1975).

Ph.D. Committee: James E. Robertson (Chair), David J. Kuck, Chuang L. (Dave) Liu, Donald B. Gillies, and Ahmed Sameh.

Professional Experience: Distinguished Professor (2010 - present), Computer Science Department, HSSEAS, UCLA;
Professor (1984 - 2010), Computer Science Department, HSSEAS, UCLA;
Department Chair (9/1/2000 - 6/30/2005);
Vice-Chair (Graduate Programs) (1995-1998, 1988-1994, 1982-1986);
Vice-Chair (Industrial Relations) (1998-1999, 2009 - present);
Associate Professor (1979-1984);
Assistant Professor (1975-1979);
Research Engineer (1966-1970), Institute for Automation and Telecommunications "M.Pupin," (Digital Laboratory), Belgrade, Yugoslavia;
Assistant Engineer (1965-1966), Brown Boveri Co., Telecommunications, Baden, Switzerland;
Consultant to: Hughes Research Laboratories, (1979-1990); Jet Propulsion Laboratory, (1978-82); U.S. government and industrial organizations (1975 - present); GMD Institute (German government), (1984-88). Hughes Aircraft Company, (1988 - 1997).

Research Theory and design of computer arithmetic algorithms: emphasis on fast division, square root and multiplication; design of fast floating-point units; complex arithmetic; on-line arithmetic, most-significant-digit-first algorithms, and composite algorithms; arithmetic structures for low power; application-specific numerical processors; reconfigurable gate arrays (FPGAs) and systems; functional (applicative) languages and architectures; digital design.

Teaching UCLA Computer Science Department: *Logic Design of Digital Systems* (CS M51A), *Computer Systems Architecture* (CS151B), *Design of Digital Systems* -

Elective (CS151C), *Advanced Computer Architecture* (CS251A), *Parallel Computer Architecture* (CS251B), *Arithmetic Algorithms and Processors* (CS252A), *Special Topics in High-Speed Computing* (CS259 - Seminar);
UCLA Extension: *High-Speed Computer Organization: Super Machines and Low-Cost Systems*, Short Course, (1979 - 1986).

Membership and Professional Services

• Life Member IEEE, (2014 - present)
• Foreign Member, Serbian Academy of Sciences and Arts, (2003 - present);
• Fellow IEEE (2003 - present);
• IEEE Computer Society (1975 - present); IEEE Technical Committee for VLSI for Signal Processing;
• ACM (1975 - present); SigARCH;
• Nikola Tesla Memorial Society, Science Committee (1985 - present);
• UCLA Engineer Advisory Board, 2001 - 2004;
• Chancellor's Advisory Board for the Crump Institute (UCLA Medical School) (1985 - 1995);
• IEEE Transactions on Computers, Editorial Board (1988-1992); • Journal of Parallel and Distributed Computing, Editorial Board (1986-1993);
• Program Committee of the IEEE Symposium on Computer Arithmetic (1978 - present); General Chair (1978); Program Co-chair (1989);
• Chair, IEEE Steering Committee on Computer Arithmetic (1999 - 2001); Member (1999- present);
• Technical Program Co-Chair, IEEE ASAP 2009. (Application-Specific Systems, Architectures and Processors;
• Member, Asilomar Conference on Signals, Systems and Computers, Steering Committee (2004 - present);
• Arithmetic Session Chair, ASILOMAR Conference, (1986, 2004, 2006, 2007);
• Arithmetic Session Chair, SPIE Conference, (1999-2001, 2003, 2004, 2009);
• Member, Technical Program Committee, FCCM, 2007 - present;
• Member, Technical Program Committee, RNC'5 (Real Numbers and Computers), 2003.

Invited Talks and Panels

• Arithmetic: Past Revisited, Acceptance presentation for receiving Medal of Ecole Normale Superieure, Lyon, France (22nd IEEE Symposium on Computer Arithmetic, 2015
• Nikola Tesla, Electrical and Computer Engineering Department, University of Texas, Dallas, March 2012;
• Omnipresence of Tesla's Work and Ideas, Electrical and Computer Engineering Department, Yale University, September 7, 2010;
• Getting More from Less: Trends in Computer Architectures, Serbian Academy of Sciences and Arts, Belgrade, September 19, 2007;
• Omnipresence of Tesla's Work and Ideas, Simon Fraser University, Burnaby, Canada, November 17, 2006;
• Omnipresence of Tesla's Work and Ideas, Serbian Academy of Sciences and Arts, Belgrade, October 18, 2006;
• Arithmetic Approaches to Bayesian Network Computations, Intel-Barcelona Lab, July 8, 2005;
• On-line Arithmetic, STMicroelectronics Lab, San Diego, August 11, 2004.
• New Models for Computer Engineering Programs, CRA Conference at Snowbird, July 12, 2004.
• Complex Arithmetic, Microsoft Research Lab, April 21, 2004;
• Fast Low-Power Multipliers, EE Department, University of Belgrade, Serbia, June 2003;

• Complex Division with Prescaling of Operands, ECE Department, University of Wisconsin - Madison, March 2003.
• Fast Arithmetic, ECE Department, George Washington University, Washington, D.C., March 2001.
• Seminar on Nikola Tesla, UC Berkeley, 2000.
• Reconfigurable Arithmetic Seminar, University of Provence, Marseilles, France, June 1999.
• Online Algorithms, Symposium on CORDIC, Technical University, Delft, Holland, March 1998.
• Redundant Arithmetic, Seminar, University of Provence, Marseilles, France, June 1998.
• Online Arithmetic, 12th Symposium on Weak Arithmetic, Metz, France, 1996.
• Approaches to Fast Arithmetic, Real Numbers and Computers, St. Etienne, France, 1995.
• Low-Power Arithmetic, University of California at Los Angeles, Computer Science Department Seminar, 1994.
• Arithmetic for Recursive Filters, Rockwell International Science Center, Thousand Oaks, May 1993.
• Online Arithmetic: Design Methodology and Application, 1992 IEEE Workshop on VLSI Signal Processing, Napa, 1992.
• Fast Arithmetic, **Distinguished Speaker**, EE Department, UC San Diego, 1991.
• On-Line Arithmetic, Ecole Normal Superieure , Lyon, France, 1991.
• Application-Specific Arithmetic Approaches, University of California at Los Angeles, Computer Science Department Seminar, 1990.
• Composite Arithmetic, University of California at Santa Cruz, Computer Science Program Seminar, 1990.
• Vector Processors, ETAN Advanced Simulation Seminar, Dubrovnik, 1990.
• High-Performance Computer Architectures, Lecture Series, Institute M. Pupin, Belgrade, 1989.
• Supercomputers, Annual Computer Society Conference, Rio de Janeiro, Brazil, 1988.
• Redundant Arithmetic, Memorial University, New Foundland, Canada, 1988.
• Fast Arithmetic, USC, EE & Systems Department Seminar, 1987.
• Parallel Architectures, Eidgenossische Technische Hochschule (ETH) Seminar, Zuerich, Switzerland, 1987.
• Supercomputer Architectures, Technical University of Berlin Seminar, 1986.
• On-Line Arithmetic and Dataflow Architectures, University of Utah, Computer Science Department Seminar, 1985.
• High-Performance Architectures, Gesellshaft fuer Mathematische Dataverarbeitung, St.Augustin-Bonn, Germany, 1984;.
• On-Line Arithmetic Algorithms, Yale University, Computer Science Department Seminar, 1983.
• Evaluation of Polynomials and Rational Functions, Ecole Superieure d'Electrotechnique et Electronique Seminar, Paris, 1983.
•, Low-Cost Processors, Special Libraries Association, Los Angeles, 1982.
• Panel, IEEE Workshop on Computer Elements, Phoenix, 1982.
• Approaches to High-Performance Architectures, Invited Speaker DATASHOW'81, Tokyo, 1981.
• On Supercomputer Architectures, Institute for Automation "M.Pupin," Belgrade, 1981.
• Dataflow Architectures, Electrical Engineering Department, University of Belgrade, 1981.
• Floating-Point On-Line Arithmetic, University of Michigan, 1980.

• Short Course on Computer Organization, IBM Santa Teresa Labs, 1979.
• A Method for Evaluating Rational Approximations, ACM SIGNUM Los Angeles Chapter Seminar, 1978.
• Panel, MIT Data-Flow Workshop,1977; MIT Data-Flow Workshop, 1978.
• Online Iterative Networks, University of Michigan, Electrical and Computer Engineering, 1976.
• Digital Arithmetic - Some New Results, Electrical Engineering Department, University of Belgrade, 1976.

Awards

• The Medal of École Normale Supérieure de Lyon, France, 2015.

• Distinguished Alumni Educator Award, Department of Computer Science, University of Illinois Urbana-Champaign, 2013.

• The Lockheed Martin Excellence in Teaching Award, 2009.

• The Okawa Foundation: Efficient Schemes for Fast Computation of Inferences in Bayesian Networks, 2006.

• Best paper award: M.D. Ercegovac and J.-M. Muller, Complex Square Root with Operand Prescaling. *IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. 293-303, 2004.

• Foreign Member of the Serbian Academy of Sciences and Arts, for contributions to theory and practice of digital arithmetic, 2003.

• IEEE Fellow, for contributions to theory and practice of digital arithmetic, 2003.

• NASA Certificate of Recognition for technical contributions to fault-tolerant computer systems, 1980.

Books, Chapters in Books, and Editorships

1. F. de Dinechin, M. D. Ercegovac, J.-M. Muller, and N. Revol, *Digital Arithmetic*, Chapter in: Wiley Encyclopedia of Computer Science and Engineering, Benjamin Wah (Ed.), New York: John Wiley & Sons, Inc., 935-948, 2008.
2. M.D. Ercegovac and T. Lang. *Digital Arithmetic* Morgan Kaufmann Publishers - an Imprint of Elsewier Science, San Francisco, 2004.
3. M.D. Ercegovac, T. Lang and J. Moreno, *Introduction to Digital Systems.*, John Wiley & Sons, (translation in Chinese), pps. 498, 2002.
4. M.D. Ercegovac, T. Lang and J. Moreno, *Introducao aos Sistemas Digitais.*, Porto Alegre, Brazil, (translation in Portuguese of Item no. 3), pps. 498, 2000.
5. M.D. Ercegovac, T. Lang and J. Moreno, *Introduction to Digital Systems.*, New York, NY: John Wiley & Sons, pps. 498, 1999.
6. M.D. Ercegovac and T. Lang. *Division and Square Root: Digit-Recurrence Algorithms and Implementations.* Norwell, MA: Kluwer Academic Publishers, pps. 230, 1994.
7. Conference paper No. 84 reprinted in *Fault-Tolerant Computing - Highlights from 25 Years*, D. Siewiorek, Editor, IEEE Computer Society Press, 1995.
8. Journal papers No. 20, 22, 24, 29, 30, and 37 reprinted in *Computer Arithmetic*, 2 Volumes, E.E. Swartzlander, Jr., Editor, IEEE Computer Society Press, 1990.
9. M.D. Ercegovac and E.E. Swartzlander (Editors), *Proceedings of the 9th IEEE Symposium on Computer Arithmetic*, pps. 247, IEEE Computer Society Press , 1989.
10. M.D. Ercegovac and D. Patel. Reduction Machines. in *High-Level Language Architectures*, Ed. V. Milutinovic, Computer Science, pp.413-429, 1988.
11. M.D. Ercegovac and T. Lang. General Approaches for Achieving High Speed Computations. in *Supercomputers*, Ed. S. Fernbach, North Holland, pp.1-28, 1986.
12. M.D. Ercegovac and T. Lang. Vector Processing. in *Supercomputers*, Ed. S. Fernbach, North Holland, pp.29-57, 1986.
13. M.D. Ercegovac and T. Lang. *Digital Systems and Hardware/Firmware Algorithms.* New York: J. Wiley & Sons, pps. 838, 1985.

Journal Publications

1. W. Yan, M.D. Ercegovac and H. Chen, An Energy-Efficient Multiplier With Fully Overlapped Partial Products Reduction and Final Addition, *IEEE Transactions on Circuits and Systems,*, 63(11):1954-1963, 2016.
2. D. Wang, J.-M. Muller, N. Brisebarre and M.D. Ercegovac, (M,p,k) - Friendly Points: A Table-Based Method to Evaluate Trigonometric Function *IEEE Transactions onCircuits and Systems II: Express Briefs*, 61(9):711-715, 2014.

3. D. Wang, M.D. Ercegovac, and Y. Xiao, Complex Function Approximation Using Two-Dimensional Interpolation, *IEEE Trans. Computers*, 63(12):2948-2960, 2014.

4. M. Ozbilen and M. D. Ercegovac, Design and evaluation of schemes for computing sum of squares in fixed point, *Turkish Journal of Electrical Engineering & Computer Sciences,* 500-512, April 2013.

5. D. Wang and M.D. Ercegovac, A Radix-16 Combined Complex Division/Square Root Unit with Operand Prescaling, *IEEE Trans. Computers*, 61(9):1243-1255, 2012.

6. P. Kulkarni, P. Gupta, and M.D. Ercegovac, Trading Accuracy for Power in a Multiplier Architecture, Journal of Low Power Electronics, Vol. 7, 1-12, 2011.

7. D. Wang, M.D. Ercegovac, and N. Zheng, Design of High-Throughput Fixed-Point Complex Reciprocal/Square-Root Unit. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 57(8):627-631, 2010.

8. M.D. Ercegovac and J.-M. Muller, An Efficient Method for Evaluating Complex Polynomials. *Journal of Signal Processing Systems*, Volume 58, Issue 1, Page 17, Springer 2010, also published online http://www.springerlink.com/content/5582844402n0t2x1/

9. Kwak, S., Lee,J-G., Jung, E-G., Har, D., Ercegovac, M.D., J-A. Lee, Exploration of Power-Delay Trade-Offs with Heterogeneous Adders by Integer Linear Programming, *Journal of Circuits, Systems, and Computers,* 18(4):787 - 800 (2009)

10. M.D. Ercegovac and J.-M. Muller, Complex Square Root with Operand Prescaling. *Journal of VLSI Signal Processing*, 49:1930, 2007.

11. J.-A. Pineiro, M.D. Ercegovac. and J.D. Bruguera, High-Radix Logarithm with Selection by Rounding: Algorithm and Implementation. *Journal of VLSI Signal Processing*, Vol.40, pp.109-123, 2005.

12. Z. Huang and M.D. Ercegovac, High-Performance Low-Power Left-to-Right Array Multiplier Design. *IEEE Trans. Computers*, 54(3):272-283, 2005.

13. J.-A. Pineiro, M.D. Ercegovac, and J.D. Bruguera, Algorithm and Architecture for Logarithm, Exponential, and Powering Computation. *IEEE Trans. Computers*, 53(9):1085-1096, 2004.

14. D. Chen, J. Cong, M.D. Ercegovac, and Z. Huang, Performance-driven mapping for CPLD architectures. *IEEE Trans. on CAD of Integrated Circuits and Systems*, Vol. 22, No. 10, pp. 1424-1431, October 2003.

15. M.D. Ercegovac and T. Lang, Comments on "A carry-free 54x54-bit multiplier using equivalent bit conversion", *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 1, pp. 160-161, 2003.

16. D. Lau, A. Schneider, M.D. Ercegovac, and J.A. Villasenor, FPGA-based library for on-line signal processing. *Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology*, 28(1-2):129-43, Kluwer Academic Publishers, May-June 2001.

17. M.D. Ercegovac, T. Lang, J.-M. Muller, and A. Tisserand, Reciprocation, Square Root, Inverse Square Root, and Some Elementary Functions Using Small Multipliers. *IEEE Trans. Computers*, 49(7):628-637, 2000.

18. M.D. Ercegovac, L. Imbert, D.W. Matula, J.-M. Muller, and G. Wei, Improving Goldschmidt Division, Square Root, and Square Root Reciprocal. *IEEE Trans. Computers*, 49(7):759-762, 2000.

19. M.R. Stan, A.F. Tenca, and M.D. Ercegovac, Long and Fast Up/Down Counters. *IEEE Trans. Computers*, 47(7):722-735, 1998.

20. J.S. Fernando and M.D. Ercegovac, A Method of Eliminating Oscillations in High-Speed Recursive Digital Filters. *IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing*, 44(10):861-864, 1997.

21. M.D. Ercegovac and T. Lang, On Recoding in Arithmetic Algorithms, *J. of VLSI Signal Processing*, 14:283–294, 1996.

22. R. Dionysian and M.D. Ercegovac. Vector Quantization with Variable-Precision Classification. *IEEE Trans. on Image Processing*, 5(11):1528–1538, 1996.

23. R. Dionysian and M.D. Ercegovac, Vector quantization with compressed codebooks. *Image Communications*, 9:79–88, 1996.

24. M. Louie and M.D. Ercegovac. A variable-precision square root implementation on field programmable gate arrays. *The Journal of Supercomputing*, 9:315–336, 1995.

25. M. Louie and M.D. Ercegovac. Implementing division with field programmable gate arrays. *J. of VLSI Signal Processing*, 7:271–285, 1994.

26. M.D. Ercegovac, T. Lang, and P. Montuschi. Very-high radix division with prescaling and selection by rounding. *IEEE Trans. Comput.*, 43(8):909–918, August 1994.

27. J.S. Fernando and M.D. Ercegovac. Conventional and on-line arithmetic designs for high-speed recursive digital filters. *J. of VLSI Signal Processing*, 7:189–197, 1994.

28. M.D. Ercegovac and T. Lang. Multiplication/division/square root module for massively parallel computers. *Integration, the VLSI Journal*, 16:221–234, 1993.

29. A. Kapelnikov, R.R. Muntz, and M.D. Ercegovac. A methodology for performance analysis of parallel computations with looping constructs. *J. of Parallel and Distributed Computing*, 14(3):105–120, March 1992.

30. L. Alkalaj, T. Lang, and M.D. Ercegovac. Architectural support for goal management in flat concurrent Prolog. *Computer*, 25(8):34–47, August 1992.

31. M.D. Ercegovac and T. Lang. On-the-fly rounding. *IEEE Trans. Comput.*, Vol. 41(12):1497–1503, Dec. 1992.

32. M.D. Ercegovac and T. Lang. Module to perform multiplication, division and square root in systolic arrays for matrix computations. *J. Parallel and Distributed Computing*, 11(3):212–221, March 1991.

33. S.-L. Lu and M. D. Ercegovac. Evaluation of two-summands adders implemented in ECDL CMOS differential logic. *IEEE J. of Solid-State Circuits*, 26(6):1152–1160, August 1991.

34. P.K.-G. Tu and M.D. Ercegovac. Gate array implementation of on-line algorithms for floating-point operations. *J. of VLSI Signal Processing*, (3):307–317, 1991.

35. S.-L. Lu and M. D. Ercegovac. A novel CMOS implementation of double-edge-triggered flip-flops. *IEEE Journal of Solid-State Circuits*, 25(4):1008–1009, August 1990.

36. M.D. Ercegovac and T. Lang. Simple radix-4 division with operands scaling. *IEEE Trans. Comput.*, Vol. C-39(9):1204–1207, Sept. 1990.

37. M.D. Ercegovac and T. Lang. Redundant and on-line CORDIC: Application to matrix triangularization and svd. *IEEE Trans. Comput.*, 39(6):725–740, June 1990.

38. M.D. Ercegovac and T. Lang. Radix-4 square root without initial PLA. *IEEE Trans. Comput.*, Vol. C-39(8):1016–1024, Aug. 1990.

39. M.D. Ercegovac and T. Lang. Fast multiplication without carry-propagate addition. *IEEE Trans. Comput.*, C-39(11):1385–1390, November 1990.

40. A. Kapelnikov, R.R. Muntz, and M.D. Ercegovac. A modeling methodology for the analysis of concurrent systems and computations. *Journal of Parallel and Distributed Computing*, 6:568–597, 1989.

41. M.D. Ercegovac and T. Lang. Fast radix-2 division with quotient-digit prediction. *J. of VLSI Signal Processing*, 2(1):169–180, Jan. 1989.

42. M.D. Ercegovac and T. Lang. Binary counter with counting period of one half adder independent of counter size. *IEEE Transactions on Circuits and Systems*, 36(6):924–926, June 1989.

43. M.D. Ercegovac and T. Lang. On-line scheme for computing rotation factors. *J. Parallel and Distributed Computing*, 5(6):209–227, June 1988.

44. M.D. Ercegovac. Heterogeneity in supercomputer architectures. *Parallel Computing*, 7:367–372, September 1988.

45. M.D. Ercegovac and T. Lang. On-the-fly conversion of redundant into conventional representations. *IEEE Trans. Comput.*, Vol. C-36(7):895–897, July 1987.

46. J.L. Gaudiot and M.D. Ercegovac. Performance analysis of variable resolution dataflow systems. *J. of Parallel and Distributed Systems*, November 1985.

47. C.S. Raghavendra, A. Avizienis, and M.D. Ercegovac. Fault-tolerance in binary tree architectures. *IEEE Trans. Comput.*, Vol. C-33(6):568–571, June 1984.

48. O. Watanuki and M. D. Ercegovac. Error analysis of certain floating-point on-line algorithms. *IEEE Trans. Comput.*, C-32(4):352–358, April 1983.

49. V.G. Oklobdzija and M.D. Ercegovac. An on-line square root algorithm. *IEEE Trans. Comput.*, Vol. C-31(1):70–75, Jan. 1982.

50. M.D. Ercegovac. A fast Gray-to-binary code conversion. *Proc. of the IEEE*, 66(4):524–525, April 1978.

51. M.D. Ercegovac. Reply on 'comments on A fast Gray-to binary conversion'. *Proc. of the IEEE*, 67(3):444–445, March 1979.

52. M.D. Ercegovac. A general hardware-oriented method for evaluation of functions and computations in a digital computer. *IEEE Trans. Comput.*, C-26(7):667–680, July 1977.

53. K.S. Trivedi and M.D. Ercegovac. On-line algorithms for division and multiplication. *IEEE Trans. Comput.*, C-26(7):681–687, July 1977.

54. M.D. Ercegovac. Radix-16 evaluation of certain elementary functions. *IEEE Trans. Comput.*, Vol. C-22(6):561–566, June 1973.

Conference Publications

1. W. Yan and M. D. Ercegovac, Radix-4 Energy Efficient Carry-Free Truncated Multiplier, *Proc. 50th Asilomar Conference on Signals, Systems and Computers*, 2016.

2. C-E. Lee and M.D. Ercegovac, An Error-Compensated Piecewise Linear Logarithmic Arithmetic Unit for Phong Lighting Acceleration, *Proc. 49th Asilomar Conference on Signals, Systems and Computers*, 2015.

3. M.D. Ercegovac and L. Meng, Low-power Radix-4 Quotient Generator, *Proc. 48th Asilomar Conference on Signals, Systems and Computers*, 2014.

4. H. Parta, M.D. Ercegovac and S. Pamarti, RF Digital Predistorter Implementation using Polynomial Optimization, IEEE 57th International Midwest Symposium on Circuits and Systems, 2014.

5. M.D. Ercegovac, On Approximate Arithmetic, *Proc. 47th Asilomar Conference on Signals, Systems and Computers*, 2013.

6. J. Cong. M.D. Ercegovac, M. Huang, S. Li, and B. Xiao, Energy-Efficient Computing Using Adaptive Table Lookup Based on Nonvolatile Memories, *Proc. International Symposium on Low Power Electronics and Design - ISLPED 2013*, 2013.

7. S. W. Heo, S. J. Huh and M.D. Ercegovac, Power Optimization of Sum-of-Products Design for Signal Processing Applications, *IEEE International Conference on Application-Specific Systems, Architectures and Processors - ASAP 2013*

8. S. W. Heo, S. J. Huh and M.D. Ercegovac, Power Optimization in a Parallel Multiplier using Voltage Islands, *Proc. ISCAS 2013*, 2013.

9. M.D. Ercegovac and R. McIlheny, Shared Implementation of Radix-10 and Radix-16 Square Root Algorithm with Limited Precision Primitives, *Proc. 46th Asilomar Conference on Signals, Systems and Computers*, 2012.

10. P. Dormiani and M.D. Ercegovac, Linearization using Efficient Complex Polynomial Evaluations, *Proc. 46th Asilomar Conference on Signals, Systems and Computers*, 2012.

11. N. Brisebarre, M.D. Ercegovac, and J.-M. Muller, (M; p; k)-friendly points: a table-based method for trigonometric function evaluation, *2012 IEEE 23rd International Conference on Application-Specific Systems, Architectures and Processors*, 2012.

12. M.D. Ercegovac and R. McIlhenny, Shared Implementation of Radix-10 and Radix-16 Division Algorithm with Limited Precision Primitives, *Proc. 45th Asilomar Conference on Signals, Systems and Computers*, 2011.

13. S. Singh, S. Pan, and M.D. Ercegovac, Accelerating the Photon Mapping Algorithm and its Hardware Implementation, *IEEE International Conference on Application-Specific Systems, Architectures and Processors - ASAP 2011*, September 2011.

14. P. Kulkarni, P. Gupta, and M.D Ercegovac, Trading Accuracy for Power with an Underdesigned Multiplier Architecture, *Proc. 24th Annual Conference on VLSI Design*, pp. 346-351, 2011.

15. M.D. Ercegovac and R. McIlhenny, Design and FPGA Implementation of Radix-10 Combined Division/Square Root Algorithm with Limited Precision Primitives, *Proc. 44rd Asilomar Conference on Signals, Systems and Computers*, 2010.

16. D. Wang, M.D. Ercegovac and N. Zheng, Design and Analysis of High Radix Complex Dividers, *Proc. The 2nd International Conference on Computer Engineering and Technology (ICCET 2010)*, 2010.

17. N. Brisebarre, N. Louvet, . Martin-Dorel, J.-M. Muller, A. Panhaleux, and M.D. Ercegovac, Implementing Decimal Floating-Point Arithmetic through Binary: some Suggestions. *IEEE International Conference on Application-Specific Systems, Architectures and Processors - ASAP 2010*, July 2010.

18. M.D. Ercegovac and R. McIlhenny, Design and FPGA Implementation of Radix-10 Algorithm for Square Root with Limited Precision Primitives, *Proc. 43rd Asilomar Conference on Signals, Systems and Computers*, 2009.

19. P. Dormiani, M.D. Ercegovac, and J.-M. Muller, Low Precision Table Based Complex Reciprocal Approximation, *Proc. 43rd Asilomar Conference on Signals, Systems and Computers*, 2009.

20. D. Wang, M.D. Ercegovac, and N. Zheng, A Radix-8 Complex Divider for FPGA Implementation, *Proc. IEEE FPL Conference*, 2009.

21. M.D. Ercegovac and R. McIlhenny, On the design of a Radix 10 online floating-point multiplier, *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations*, August 2009.

22. D. Wang and M.D. Ercegovac, A Design of Complex Square Root for FPGA Implementation, *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations*, August 2009 .

23. P.D. Dormiani, M.D. Ercegovac, and J.-M. Muller, Design and Implementation of a Radix-4 Complex Division Unit with Prescaling, *IEEE International Conference on Application-Specific Systems, Architectures and Processors - ASAP 2009*, July 2009.

24. P. Dormiani and M.D. Ercegovac, Design and Implementation of Complex Multiply Add and Other Similar Operators. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XVIII*, Vol. 7074, 12 pps., 2008.

25. M.D. Ercegovac and R. McIlhenny, Design and FPGA Implementation of Radix-10 Algorithm for Division with Limited Precision Primitives. *Proc. 42nd Asilomar Conference on Signals, Systems and Computers*, pp. 1-5, 2008.

26. N. Brisebarre, S. Chevillard, M. D. Ercegovac, J.-M. Muller and S. Torres. An Efficient Method for Evaluating Polynomial and Rational Function Approximations. *IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. 233-238, July 2008.

27. T.Y. Yeh, P. Faloutsos, M.D. Ercegovac, S.J. Patel, and G. Reinman. The Art of Deception: Adaptive Precision Reduction for Area Efficient Physics Acceleration. 40th Annual IEEE/ACM International Symposium on Microarchitectures, MICRO-07, pp. 394-406, 2007.

28. J-G. Lee, J-A. Lee, B-S. Lee, and M.D. Ercegovac, A Design Method for Heterogeneous Adders, Proc. ICESS 2007, Lecture Notes in Computer Science 4532, pp. 121-132, Springer-Verlag, 2007.

29. M.D. Ercegovac. On Digit-by-Digit Methods for Computing of Certain Functions. *Proc. 41st Asilomar Conference on Signals, Systems and Computers*, pp. 338-342, 2007.

30. P. Dormiani and M.D. Ercegovac, ISA Extensions for Online Floating-Point Addition. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, Vol. 6697, 12 pps., 2007.

31. M.D. Ercegovac and J.-M. Muller, Complex Multiply-Add and Other Related Operators. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, Vol. 6697, 12 pps., 2007.

32. M.D. Ercegovac and J.-M. Muller, A Hardware-Oriented Method for Evaluating Complex Polynomials. *IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. 122-127, 2007.

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