Why Analog-to-Information Converters Suffer in High-Bandwidth Sparse Signal Applications

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***Abstract*—In applications where signal frequencies are high, but information bandwidths are low, analog-to-information converters (AICs) have been proposed as a potential solution to overcome the resolution and performance limitations of high-speed analog-to-digital converters (ADCs). However, the hardware implementation of such systems has yet to be evaluated. This paper aims to fill this gap, by evaluating the impact of circuit impairments on performance limitations and energy cost of AICs. We point out that although the AIC architecture facilitates slower ADCs, the signal encoding, typically realized with a mixer-like circuit, still occurs at the Nyquist frequency of the input to avoid aliasing. We illustrate that the jitter and aperture of this mixing stage limit the achievable AIC resolution. In order to do so, we designed an end-to-end system evaluation framework for examining these limitations, as well as the relative energy-efficiency of AICs versus high-speed ADCs across the resolution, receiver gain and signal sparsity. The evaluation shows that the currently proposed AICs have no performance benefits over high-speed ADCs. However, AICs enable 2–10X in energy savings in low to moderate resolution (ENOB), low gain applications.**

***Index Terms*—Analog-to-digital converter (ADC), analog-to-information converter (AIC), compressed sensing (CS).**

I. Introduction

EFFICIENT, high-speed samplers are essential for building modern electronic systems. One such system is cognitive radio, which has been proposed as an intelligent wireless communication protocol for improving the utilization of un-used bandwidth in the radio spectrum [1]. To implement this protocol, the entire radio spectrum has to be simultaneously observed in order to determine the location of used channels. A straightforward approach is to utilize a wideband, Nyquist rate high speed analog-to-digital converter (ADC), however, a severe drawback is that ADCs operating at multi-Giga samples per second (GS/s) require high power and have limited bit resolution [2], [3]. An alternative approach is to utilize an analog-to-information converter (AIC) based on compressed sensing (CS) techniques [4]–[12]. AICs can be used for any type of signals, which are sparse in some domain. CS is a method for recovering sparse signals from samples taken at sub-Nyquist rates [13], [14]. Consequently, AICs can relax the frequency requirements of ADCs, potentially enabling higher resolution and/or lower power receiver front-ends.

The aim of this work is to compare the energy/performance design space of AICs to that of the high-speed ADCs, in the presence of the same circuit impairments that limit the high-speed ADC performance. We explore how jitter and aperture impairments, which commonly limit ADC performance at high sampling frequencies, also impact AIC performance. Building on the AIC jitter models used in [8], we also include aperture effects. We illustrate, from a performance standpoint, that AICs do not enable higher effective number of bits (ENOB), as compared to a baseline high-speed ADC system. However, they may consume less power, depending on the nature of the input signal such as signal sparsity, and some other factors such as the required receiver gain. We also illustrate that counter-intuitively, using sparse sampling matrices does not help mitigate jitter effects, when compared to dense sampling matrices. We illustrate these insights using a cognitive radio example, with 1000 channels that span the 500 MHz–20 GHz frequency spectrum. This evaluation methodology can be extended in a fairly straightforward manner to other sparse signal applications.

The remainder of the paper is organized as follows. Section II begins with a brief introduction to high-speed sampler limitations and describes a currently proposed AIC system. In Section III, we describe the system evaluation framework which incorporates signal and noise models, and CS reconstruction. Section IV discusses the impact of jitter noise and aperture on both high-speed ADC and AIC system and describes the potential benefit of using sparse versus dense sampling matrices. Energy evaluation results and power models for an implementation of AIC and high-speed ADC systems are provided in Section V.

II. Background

A. Limitations in High-Speed Sampling

To date, high-speed samplers are used in most modern electronic systems [2]. These systems, which work on a variety of signals such as speech, medical imaging, radar, and telecommunications, require high-speed samplers such as high-speed ADCs, to have high bandwidth and significant resolution while working at high frequencies (10's of GS/s). Unfortunately, with the current technology, designing high resolution ADCs is quite challenging at such high frequencies. This is mainly due to the fact that these samplers are required to sample at the Nyquist rate (i.e., at least twice the highest frequency component in the signal) to be able to recover the original signal without any loss.

Manuscript received June 18, 2012; revised October 09, 2012; accepted January 05, 2013. Date of publication February 26, 2013; date of current version August 26, 2013. This work was supported in part by the National Science Foundation (NSF) Award ECCS 1128226 and the National Science and Engineering Research Council of Canada (NSERC). This paper was recommended by Associate Editor S. R. Sonkusale.

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Digital Object Identifier 10.1109/TCSI.2013.2246212

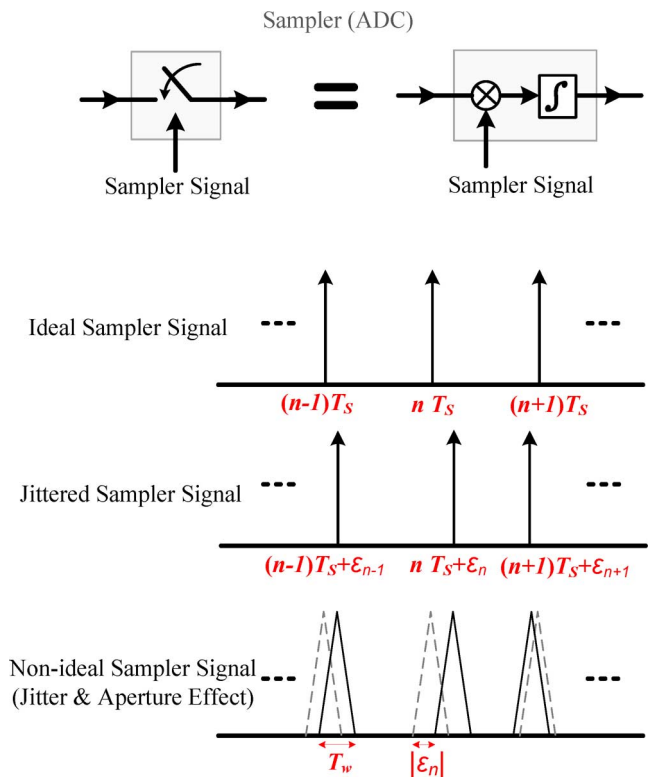

Fig. 1. Ideal and non-ideal sampler, including jitter and aperture effects.

Ideally, each sampling event should result in the signal value at the specific sampling instant. However, in practice, there are two main factors that limit the ADC performance: i) uncertainty in the sampling instant, i.e., jitter, and ii) the finite sampling bandwidth, manifested as a weighted integration over a small time interval around the sampling instant, i.e., aperture [15], [16].

As Fig. 1 shows, the sampling process consists of multiplying the input signal with some sampling signal, and then low pass filtering. The ideal sampling signal would be a delta train with impulses evenly spaced apart at sampling intervals T_S. The non-idealities of the sampling signal, e.g., jitter, are manifested through uneven spacing of sampling impulses. The nth sampling error is given by the difference of two signal values, respectively taken at times nT_s and $nT_s + \varepsilon_n$, where ε_n is a random variable that represents the nth jitter value. The jitter effect becomes more serious at higher input signal frequencies, as the signal slew-rate (i.e., rate of change of a signal) is proportional to the signal frequency. Thus, a small jitter can cause a significant error in high-speed sampling [3]. We go on to allow the non-ideal sampler signal to further incorporate aperture effects (in addition to the previously described jitter effects). This is also illustrated in Fig. 1. We model the aperture effect by replacing the delta impulses in the sampler signal with triangle pulses, where the area under the triangle is unity. In reality, the aperture in the sampler is caused by two circuit non-idealities: i) low-pass filtering of the sampler (i.e., limited sampler bandwidth in the signal path), and ii) non-negligible rise/fall time of the clock signal (sampling signal). These non-idealities make the sampler band-limited and cause significant error at high frequencies [17].

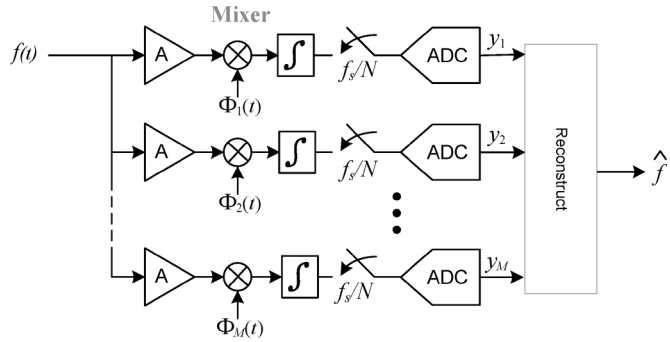

Fig. 2. Block diagram of an AIC system.

CS has enabled alternative solutions to high-speed ADCs. A well-known example is the AIC. It has been claimed that these AIC architectures enable high resolution at high frequencies while only using low frequency, sub-Nyquist ADCs [4]–[12]. In this work, we investigate whether or not AIC systems can indeed resolve both jitter and aperture issues in high-speed samplers, by examining their performance in the presence of these non-idealities.

B. Analog-to-Information Converter (AIC)

While there have been many theoretical discussions on AIC systems in the literature [4]–[12], to our knowledge, an actual hardware implementation of an AIC system working for wide signal bandwidth (10's of GHz), is yet to be seen. Hence, it is difficult to make a fair hardware-to-hardware comparison with other already implemented high-speed ADCs. Although, there are many examples of AICs [4]–[12], [18]–[20], in this work, the generic AIC circuit architecture shown in Fig. 2 is considered to be compared with a baseline high-speed ADC. In this architecture, the input signal $f(\mathrm{t})$ is amplified by using M number of amplifiers. Each signal branch is then individually multiplied with a different pseudorandom number (PN) waveform $\Phi_i(\mathrm{t})$ to perform CS-type "random" sampling. The multiplication with the PN waveform is at Nyquist rate to avoid aliasing in this stage, which we call the mixing stage. At each branch, the mixer output is then integrated over a window of N sampling periods T_S. Finally, the integrator outputs are sampled and quantized to form the measurements y_i which are then used to reconstruct the original input signal $f(\mathrm{t})$. Note that because we now sample at the rate f_s/N (see Fig. 2), this AIC architecture employs sub-Nyquist rate ADCs, which are less affected by jitter noise and aperture. The actual advantage over standard ADCs is really unclear until experimentally justified. Also, it is important to point out that the mixing stage still works at the Nyquist frequency, and circuit non-idealities such as jitter and aperture can still be a potential problem in the mixing stage in a manner similar to the sampling circuit in high-speed ADCs. In the following section we present our framework for investigating the impacts of mixer jitter and aperture on AIC performance.

III. Evaluation Framework

Fig. 3(a) shows the block diagram of the AIC system indicating the location of injected noise due to the jitter and aperture.

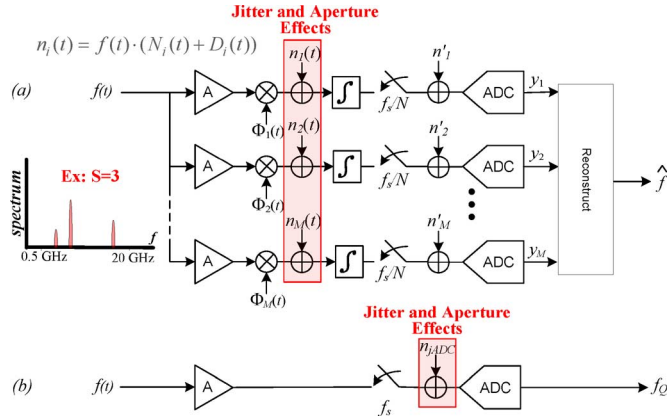

Fig. 3. Jitter effects in sampling: block diagram of (a) an AIC system, and (b) a high-speed ADC system both with same functionality in the cognitive radio setting.

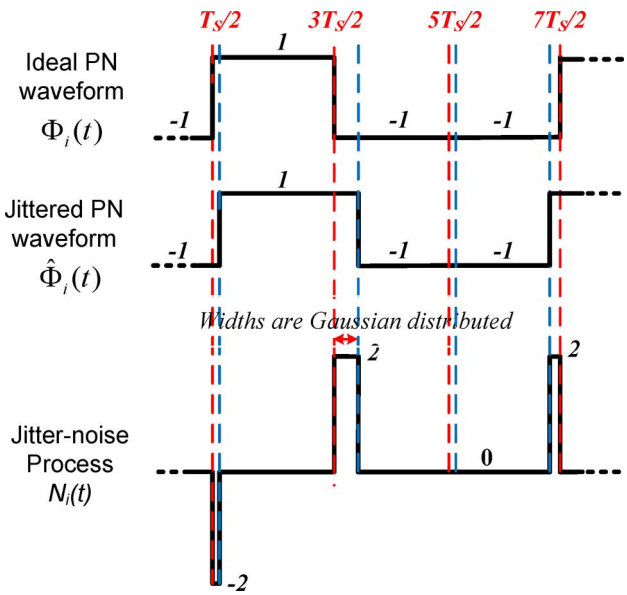

Fig. 4. Ideal and jittered PN waveforms.

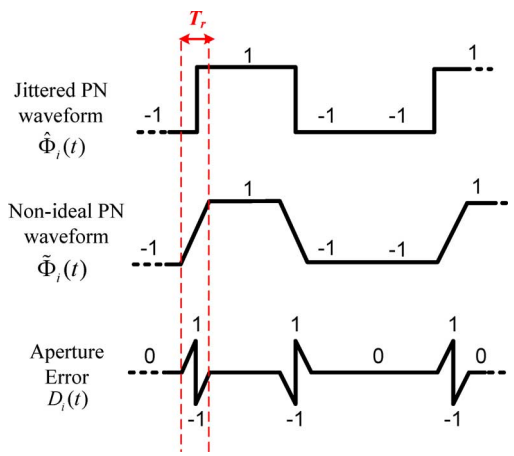

Fig. 5. Aperture error caused by non-ideal PN waveform.

Fig. 3(b) shows the same functionality of the AIC system implemented simply using an amplifier and an ADC operating at the Nyquist-rate (N times that of Fig. 3(a)). This is the system referred to as the high-speed ADC system, which also suffers from jitter and aperture effects, as illustrated in Fig. 3(b). The potential advantages of using AICs stem from having a different sensitivity to sources of aperture error and jitter introduced by different control signals in the AIC system. In the AIC system, the jitter error from sampling clocks on the slower ADCs, denoted $n_i'(t)$, is negligible, whereas the main source of error, denoted $n_i(t)$, comes from the mixer aperture and the jitter in the PN waveform mixed with the input signal at the Nyquist frequency. On the other hand, in the high-speed ADC system, the main source of error is due to the sampling jitter in the high-speed clock. In this section, we provide signal and noise models used to evaluate the performance of these two systems.

A. Signal Model

The signal model

$$f(t) = \sum_{j=1}^{N_{\rm ch}} x_j \sin(\omega_j t) \tag{1}$$

consists of transmitted coefficients, x_j, riding on the carriers with frequencies ω_j (chosen from $N_{\rm ch}$ available channel frequencies in the range of 500 MHz–20 GHz). This model emulates sparse narrowband or banded orthogonal frequency-division multiplexing communication channels [21]. Our sparsity assumption states that only S out of $N_{\rm ch}$ coefficients x_j are non-zero, i.e., only S users are "active" at any one time.

B. Mixer Clocking Jitter

Fig. 4 shows our jitter noise model where the noise is multiplied by the input signal and filtered in the integrator block. The ith PN waveform $\Phi_i(t)$ satisfies

$$\Phi_i(t) = \sum_{j=1}^{N} \phi_{ij} p(t - jT_s) \tag{2}$$

where $\phi_{\iota j}$ is the (i,j)th PN element, and $p(t)$ is a unit height pulse supported on—$T_s/2$ to $T_s/2$. Denoting the jittered PN waveform as $\hat{\Phi}_i(t)$, then: $\hat{\Phi}_i(t) = \Phi_i(t) + N_i(t)$. Here, $N_i(t)$ is the jitter noise affecting $\hat{\Phi}_i(t)$, described as

$$N_i(t) = \sum_{j=1}^{N+1} (\phi_{ij-1} - \phi_{ij}) \mathrm{sgn}(\varepsilon_j) \hat{p}_j \left(t - jT_s + \frac{T_s}{2}, \varepsilon_j \right) \tag{3}$$

where the jth jitter width is $\varepsilon_j \sim N(0,\sigma)$ with σ equal to the jitter root-mean-square (rms), and $\hat{p}_j(t,\varepsilon)$ is a unit amplitude pulse supported over the interval $[\min(0,\varepsilon), \max(0,\varepsilon)]$. To verify (3), consider the first transition in the ith PN waveform $\Phi_i(t)$ in Fig. 4, where ϕ_{i0} and ϕ_{i1} are -1 and 1, respectively. As it is shown, the jitter value ε_1 at that transition happens to be positive (i.e., PN waveform is shifted to the right due to jitter). Hence, by using (3), the jitter noise $N_i(t)$ at that transition is a pulse with a width of ε_1 and an amplitude of minus two located at $T_S/2$.

As a side comment, note that in our model for $N_i(t)$, we assumed that the same phase-locked loop (PLL) is used across all signal paths, resulting in the exact same jitter sequence ε_j for all

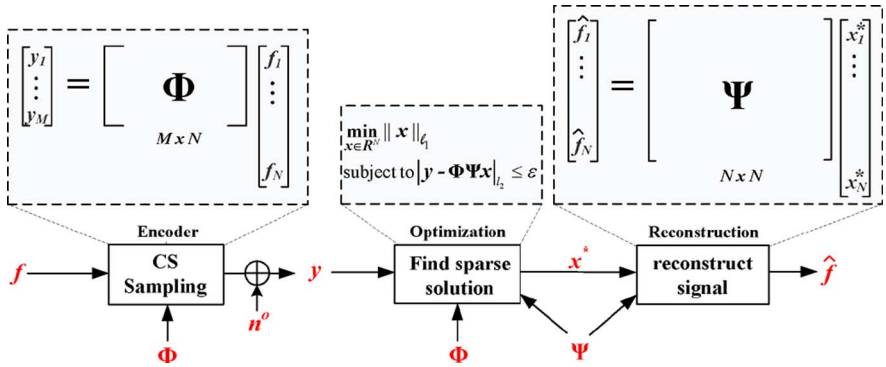

Fig. 6. Compressed sensing (CS) framework.

jittered PN waveforms $\hat{\Phi}_i(t), 1 \leq i \leq M$. This model can be extended to include the effect of a longer clock tree distribution, by adding an uncorrelated (or partially correlated) component to each branch, i.e., we would then have a different jitter sequence for each PN waveforms $\hat{\Phi}_i(t)$.

C. Aperture Models

In the AIC system, the aperture is caused by two circuit non-idealities: i) mixers do not operate instantaneously, and ii) the PN waveforms are not ideal. Fig. 5 illustrates our aperture error model, whereby the aperture effects are captured by the limited rise and fall times in the PN waveform. The aperture error, $D_i(t)$, corresponding to the ith non-ideal PN waveform $\tilde{\Phi}_i(t)$, is taken with respect to the ith jittered PN waveform $\hat{\Phi}_i(t)$, i.e., $\tilde{\Phi}_i(t) = \hat{\Phi}_i(t) + D_i(t)$. We emphasize that the reference point for the aperture error is the jittered PN waveform, not the ideal waveform (as was for the jitter noise $N_i(t)$). The formula for the ith aperture error $D_i(t)$ is given as

$$D_i(t) = \sum_{j=1}^{N+1} \left(\frac{\phi_{ij} - \phi_{ij-1}}{2} \right) q\left(t - jT_s + \frac{T_s}{2} + \varepsilon_j \right) \tag{4}$$

where ϕ_{ij} is the (i,j)th PN element, and $q(t)$ can be described as

$$q(t) = \begin{cases} \left(\frac{2t}{T_r} + 1\right) & -\frac{T_r}{2} < t \leq 0 \\ \left(\frac{2t}{T_r} - 1\right) & 0 < t < \frac{T_r}{2} \\ 0 & \text{otherwise} \end{cases} \tag{5}$$

where T_r is the parameter that dictates the rise/fall time of the PN waveform. Similar to the jitter noise, the aperture error $\mathrm{D}_i(t)$ is also multiplied by the input signal and filtered in the integrator block.

D. Reconstruction of Frequency Sparse Signal

In this section, for the sake of readers unfamiliar with CS techniques, we first provide a brief background discussion, and then we frame the reconstruction problem for the CS-based AIC system.

Signals are represented with varying levels of sparsity in different domains. For example, a single tone sine wave is either represented by a single frequency coefficient, or an infinite number of time-domain samples. Consider signals $\boldsymbol{f}$ represented as follows

$$\boldsymbol{f} = \Psi \boldsymbol{x} \tag{6}$$

where $\boldsymbol{x}$ is the coefficient vector for $\boldsymbol{f}$, which is expanded in the basis $\Psi \in \mathrm{R}^{N \times N}$. We say the signal $\boldsymbol{f}$ is sparse when most of the corresponding coefficients x_i are zero, or they are small enough to be ignored without much perceptual loss. Also $\boldsymbol{f}$ is called S-sparse when only S of the x_i coefficients have significant values.

The CS framework is shown in Fig. 6, where an N dimensional input signal $\boldsymbol{f}$ is compressed to M measurements $\boldsymbol{y}$, by taking M linear random projections, i.e.,

$$\boldsymbol{y} = \Phi \boldsymbol{f} + \boldsymbol{n}^o \tag{7}$$

where $\boldsymbol{\Phi} \in \mathrm{R}^{M \times N}, \boldsymbol{f} \in \mathrm{R}^{N \times 1}$, and $\boldsymbol{n}^o$ is a noise vector. Note that M and N respectively appear as the number of signal branches, and the integration length, in the AIC architecture in Fig. 2. In the case that $M < N$, the system is undetermined, which means there are infinite number of solutions for $\boldsymbol{f}$. However, if the signal is known *a-priori* to be sparse, under certain conditions, the sparsest signal representation satisfying (7) can be shown to be unique.

Furthermore, solving the following convex program

$$\min_{x \in R^N} \|x\|_{l_1} \text{ subject to} |\boldsymbol{y} - \Phi\Psi\boldsymbol{x}|_{l_2} \leq \varepsilon \tag{8}$$

can be shown to produce a good approximation for the original signal [13], [14], where ε accommodates for the noise $\boldsymbol{n}^o$ in (7).

Using the described CS framework, we now frame the reconstruction problem for the AIC. As Fig. 3(a) shows, each measurement y_i is computed by integrating the noise, $n_i(t) = f(t) \cdot (N_i(t) + D_i(t))$, and the product of the signal $f(t)$ and the PN waveform $\Phi_i(t)$, as follows

$$y_i = \int_{T_s/2}^{N \cdot T_s + T_s/2} f(t) \cdot \Phi_i(t) dt + \int_{T_s/2}^{N \cdot T_s + T_s/2} n_i(t) dt. \tag{9}$$

Substituting the signal model from (1), the measurements can be shown to satisfy $\boldsymbol{y} = \Phi\Psi\boldsymbol{x} + \boldsymbol{n^o}$, where PN matrix Φ has

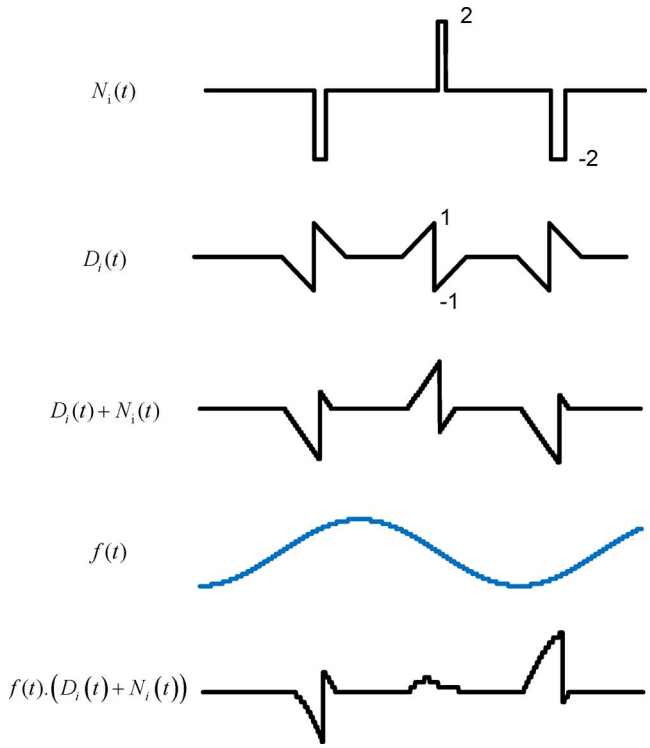

Fig. 7. Jitter noise and aperture error for a single tone sine wave.

entries ϕ_{ij} and

$$\Psi_{ij} = \int_{(i-1)\cdot T_s+T_s/2}^{i\cdot T_s+T_s/2} \sin(\omega_j t)dt, \text{ and}$$

$$n_i^o = \int_{T_s/2}^{N\cdot T_s+T_s/2} n_i(t)dt$$

$$= \int_{T_s/2}^{N\cdot T_s+T_s/2} f(t)\cdot(N_i(t)+D_i(t))dt \qquad (10)$$

where $\boldsymbol{n}^o = (n_1^o, n_2^o, \ldots, n_M^o)^T$. Here, the noise n_i^o is merely the projection of $f(t)$ by the ith jitter noise pulse process $N_i(t)$ and ith aperture error pulse $D_i(t)$ (see Figs. 4 & 5). Fig. 7 depicts the jitter noise and aperture error for a single tone sine wave input signal.

The jitter and aperture noise $\boldsymbol{n}^o$ in (10) is signal-dependent and possibly far from Gaussian, but in reconstruction (8) we favor l_2-*norm* constraints for simplicity. We use the Lasso-modified LARS algorithm [23] to solve (8). Appendix I gives more details on the exact reconstruction method used. In the next section, we use our noise model and reconstruction framework to compare the performance of AIC versus high-speed ADC systems.

IV. Evaluation Results

For our signal $f(t)$, refer to model (1), we assume 1000 possible subcarriers (i.e., $N_{\text{ch}} = 1000$). We test our system using a randomly generated signal $f(t)$, where S non-zero values are drawn from a uniform random distribution over [0, 1] to assign the information coefficients x_i, and S integer values are drawn from a uniform random distribution over $[1, N_{\text{ch}}]$ to assign subcarrier (channel location) of S active users.

To compare the performance of the high-speed ADC and the AIC systems, we adopt the same ENOB metric from the ADC literature, which is defined as [22]

$$\text{ENOB} = \log_2\left(\frac{V_{\text{swing}}}{|\boldsymbol{f} - \widehat{\boldsymbol{f}}\,|_2 \cdot \sqrt{12}}\right) \qquad (11)$$

where V_{swing} is the full-scale input voltage range of the ADCs and $|f - \hat{f}|_2$ is the rms signal distortion (use f_Q in place of $\hat{f}$ for the high-speed ADC system in Fig. 3(b)). Note that $\hat{\boldsymbol{f}}$ is the reconstructed signal at the output of the AIC system and f_Q is the quantized signal at the output of the high-speed ADC system. The actual evaluation code is now available at [24]. In order to illustrate the relative impact of jitter and aperture, we first ignore aperture effects, and limit our evaluation results to only jitter limited systems. We later add aperture effects to the jitter noise, and observe the differences.

A. Jitter-Limited ENOB

The jitter-limited ENOB for both systems is plotted in Fig. 8, parameterized by the sparsity of the signal. As the number of non-zero components of $\boldsymbol{x}(S)$ increases, we see that the AIC performance worsens while the high-speed ADC performance improves. The reasons for this are as follows. In the receiver, the input signal $f(t)$ peaks are always normalized to V_{swing}, the full-scale voltage range of the ADC. When S increases, this normalization causes the coefficient values $|x_j|$ to get smaller with respect to V_{swing}. In the high-speed ADC system, the jitter-error $|f - f_Q|_2$ is dominated by the coefficient $|x_j|$ corresponding to the highest input frequency and the error drops if the coefficient value drops. Hence, ENOB increases since $V_{\text{swing}}/|f - f_Q|_2$ increases with S, see (11). On the other hand, the AIC system has a different behavior. As S increases, the reconstruction performs worse and as a result AIC distortion $|f - \hat{f}|_2$ gets worse, resulting in poorer ENOB performance.

As shown in Fig. 8, when we consider only the impact of jitter, the AIC system can improve the ENOB by 1 and 0.25 bits for S of 1 and 2, respectively. For signals with higher S, the high-speed ADC performs better than the AIC system. As a point of reference, the standard Walden curve [3] is also plotted in Fig. 8, which depicts the ADC performance with input signal at Nyquist frequency. We see that compared to the Walden curve, the high-speed ADC can actually achieve a better resolution (i.e., the Walden curve is a pessimistic estimate). This is due to the fact that the input signal, $f(t)$, does not always have all its spectra concentrated at the Nyquist frequency, and therefore, in the real-use case, the performance of high-speed ADC is much better than the worst-case prediction of the Walden curve.

[1]normalized sampling rate is defined as $f_{\text{cs}}/f_{\text{nyq}}$, where f_{nyq} is the nyquist sampling rate, and f_{cs} is equal to M (number of parallel path) times f_{ADC} (ADCs' sampling rate in the AIC system). In our evaluations, $f_{\text{nyq}} = 40$ GHz, $M = 100$ and $f_{\text{ADC}} = 40$ MHz.

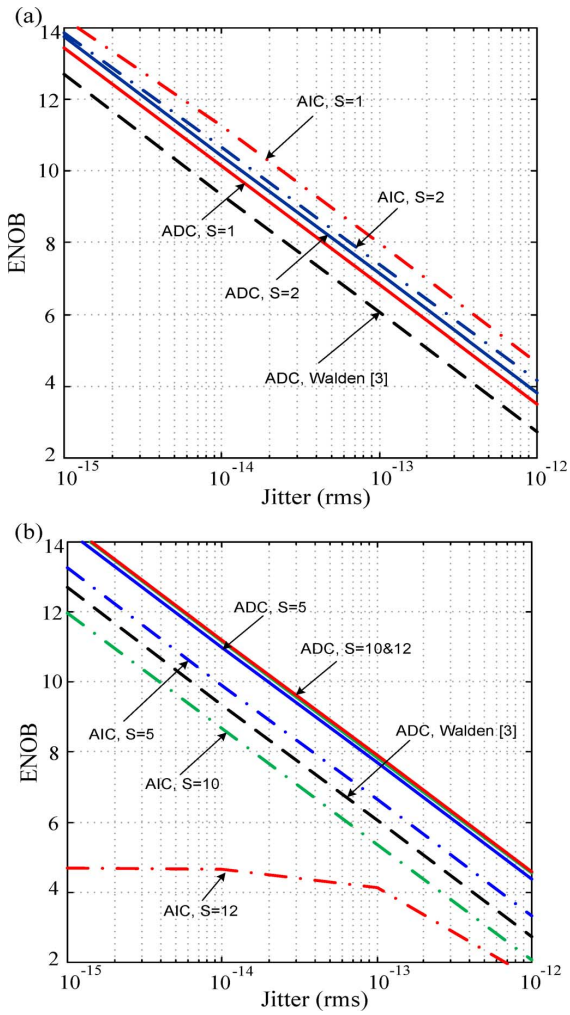

Fig. 8. Jitter (rms) versus ENOB for (a) $S = 1$ & 2 (i.e., sparsity of 0.1% and 0.2%, respectively), and (b) $S = 5, 10$ & 12 (i.e., sparsity of 0.5%, 1% and 1.2%, respectively). N, M and normalized sampling rate are 1000, 100 and 0.1, respectively, for all S.[1]

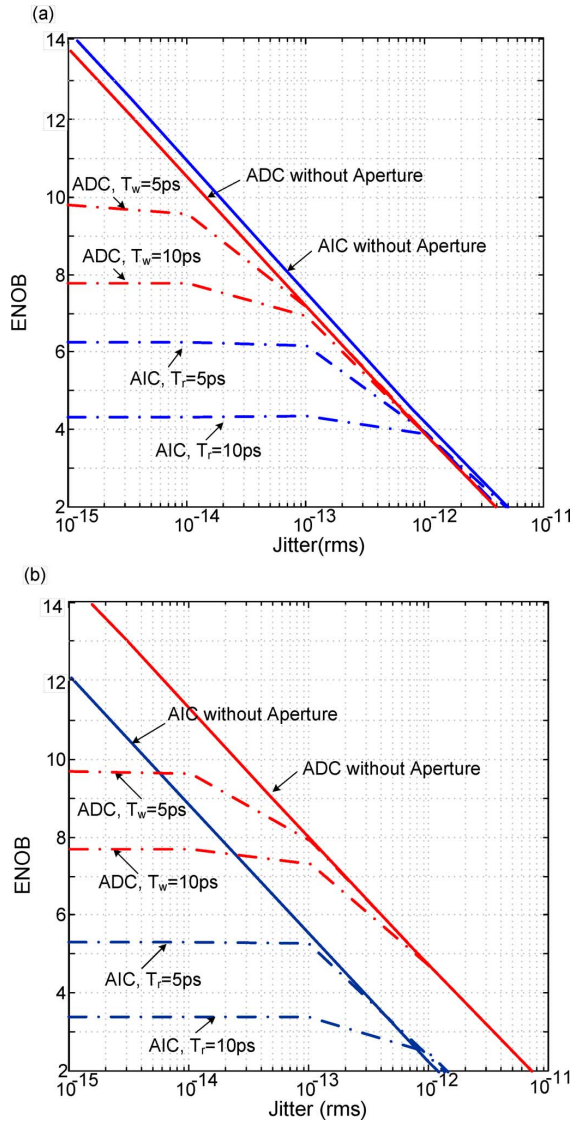

Fig. 9. Performance of the AIC system versus the high-speed ADC system including aperture and jitter effects for (a) $S = 2$, and (b) $S = 10 (N = 1000, M = 100)$.

B. *Effect of Aperture*

So far, we assumed that both the mixer and the ADC have unlimited bandwidth, i.e., we ignore the aperture effects. However, in practice, they are indeed band-limited, and this non-ideality may significantly impact their performance at high frequencies. Fig. 9(a) shows the effect of aperture on the performance of both the AIC and the high-speed ADC when $S = 2$. The high-speed ADC system performance is shown for T_w value of 5 and 10 ps, where T_w stands for the integration period in the ADCs (i.e., width of the triangle in the sampler signal, see Fig. 1). We chose these values for T_w, as they are equivalent to ADCs with 64 GHz signal bandwidth (i.e., about three times of highest input signal frequency) and 128 GHz signal bandwidth. As Fig. 9 shows, aperture can worsen the performance of the high-speed ADC system when the jitter is really small. However, as the jitter becomes bigger, it becomes the dominant source of error, diminishing the aperture effect. For comparison, the AIC performance is shown in the same figure for T_r of 5 and 10 ps, where here T_r is the rise/fall time in PN sequence waveform, see Fig. 5. The rise time of 5–10 ps is consistent with the performance of a state-of-the-art PN sequence generator [25], [26]. As Fig. 9 shows, aperture in the mixer stage can also significantly worsen the performance of the AIC system. For example, even for the extremely optimistic circuit scenario with $T_r = 5$ ps and jitter $(\text{rms}) = 10^{-14}$ s, the aperture caused the AIC performance (ENOB) to drop from 11 bits to 6 bits. Finally, we perform the same evaluation for higher number of nonzero signal components, $S = 10$, as shown in Fig. 9(b). Similar jitter and aperture limitations are also observed at the higher S value. However, as S increases, the performance of the AIC system worsens due to reconstruction limitations [27].

These aperture effects can be somewhat compensated by utilizing various adaptation or calibration techniques, for example forward calibration scheme or direct training [28], [29]. However, in reality, the compensation effect is limited by the accuracy of the estimates corrupted by jitter and AWGN noise. This effect is illustrated in Fig. 10, where we show that using direct training to deal with circuit's non idealities does not improve the performance all the way back to that of the system with ideal

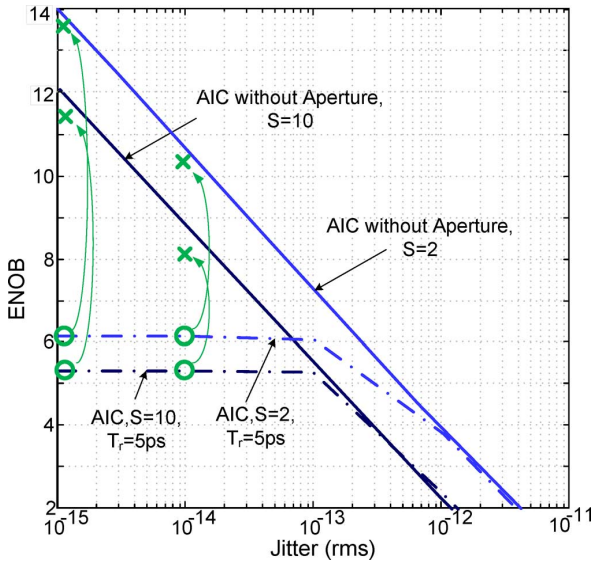

Fig. 10. Performance improvement of the AIC system by using calibration algorithms. 'O' and 'X' symbols show the results before and after calibration, respectively.

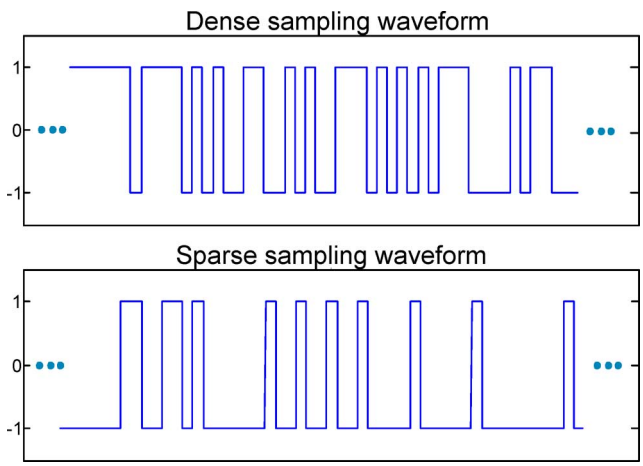

Fig. 11. Dense sampling waveform versus sparse sampling (the latter has roughly 60% less transitions).

aperture (i.e., without aperture error). The extent of the residual error depends on the AWGN and jitter accumulated during the training.

C. Sparse Sampling Matrix

Dense sampling matrices (that mix the input signal) are commonly used for CS-based signal-acquisition systems. However, sparse matrices are also a viable option [30], [31], whereby using sparse matrices can potentially relax memory requirements. Another potential benefit of sparse matrices is that the injected jitter noise at the mixer stage becomes smaller and it may potentially improve AIC performance. This is due to the fact that jitter occurs only when a transition occurs in the sampling waveform, and waveforms made from sparse matrices have fewer transitions. Fig. 11 shows sampling waveforms generated from dense and sparse matrices.

In this section, we examine whether or not sparse matrices can really allow the AIC system to be more jitter-tolerant. Using

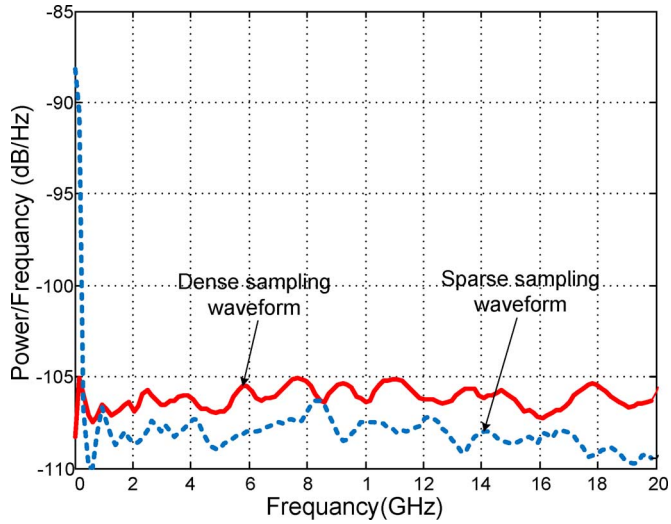

Fig. 12. Power spectral densities of both dense and sparse sampling waveforms.

a sparse sampling matrix Φ, we generated similar figures to 8 and 9 as in Subsection IV-B. We find that empirical results did not improve at all. This is due to the fact that even though the sparse waveforms made the noise smaller, they also made measurements y_i smaller, and as a result the measurement SNR is not improved at all and AIC performance stays the same. Intuitively this makes sense. Consider a high frequency, pure tone input, and some sampling waveform. In the frequency domain, the spectrum of the sampling waveform convolves with that of the single tone (at high frequency), and a shifted version of the sampling waveform spectrum will be created. The integration block attenuates high frequency and only passes the spectrum of the (shifted) sampling waveform that is located near DC. Now the frequency content of the (shifted) sampling waveform near DC is simply the frequency content of the non-shifted sampling waveform at some high frequency. Hence, only if the original (non-shifted) waveform had large frequency components at that high frequency, then bigger measurements will be seen at the output of the integrator. However, observe Fig. 12, which plots the power spectrum densities of both sparse and dense sampling waveforms (both waveforms normalized to have the same energy). Notice that at high frequencies, sparse sampling waveforms have lower power than dense sampling waveforms. Hence, the sparse sampling waveforms will generate smaller measurements. In summary, sparse sampling matrices will simultaneously degrade both signal and noise and as a result do not improve the AIC performance.

D. Performance Evaluation Summary

In conclusion, both AIC and high-speed ADC systems suffer from jitter and aperture non-idealities. For the high-speed ADC system, these non-idealities appear in the sampling stage, while for the AIC system, they appear in the mixing stage. Both jitter and aperture are frequency dependent, and since the mixer stage is still required to work at the Nyquist frequency this stage limits AIC performance in high bandwidth applications. To make matters worse, the AIC system performance degrades when the number of signal components, S, increases. This contrasts with

high-speed ADC performance, where at a higher S the performance improves (recall that this is due to a different scaling up to V_{swing}). Finally, we also investigated sparse sampling matrices, where we found that while intuition may suggest the opposite, sparse sampling waveforms are still as susceptible to jitter and aperture, as compared to dense sampling matrices.

V. Energy Cost of High-Speed ADC and AIC

In this section, we evaluate and compare the powers of both the AIC and high-speed ADC systems. Recall that AIC systems use slower-rate, sub-Nyquist ADCs, whereby the rate reduction in ADCs will result in some power savings. However, do note that the AIC architecture employs not one, but multiple ADCs, and also requires other circuits such as the integrator and mixer. Hence, it is not immediately clear if the AIC system is more power-efficient than the high-speed ADC system. In addition to the front-end, the AIC requires a reconstruction block. The cost of this block varies based on the reconstruction algorithm used. For example, in [32], we show that the energy-cost of relatively simple Matching Pursuit (MP) algorithm is comparable to the high-speed ADC energy-cost. The remaining question is the comparison of the front-end costs, so in this paper, we focus on the front-end power models. Here, we first provide power models for both high-speed ADC and AIC systems and then we use these models to analyze the relative energy efficiency of both AIC and high-speed ADC systems, across important factors such as resolution, receiver gain and signal sparsity.

These power models $P_{\text{ADC,sys}}$ and $P_{\text{AIC,sys}}$ are first given (derivation follows later) as follows

$$P_{\text{ADC,sys}} = 2\text{BW}_f \left[\underbrace{\text{FOM} \cdot 2^{\text{ENOB}}}_{\text{ADC}} + \underbrace{3C_1 \cdot G_A^2 \cdot 2^{2\text{ENOB}}}_{\text{amplifier}} \right], \text{ and} \tag{12}$$

$$P_{\text{AIC,sys}} = 2\text{BW}_f \left[\underbrace{\frac{M}{N} \cdot \text{FOM} \cdot 2^{\text{ENOB}}}_{\text{ADCs}} + \underbrace{M \cdot C_2}_{\text{integrators}} + \underbrace{\frac{M \cdot N}{4} \cdot 3C_1 \cdot G_A^2 \cdot 2^{2\text{ENOB}}}_{\text{amplifiers}} \right] \tag{13}$$

where BW_f is signal bandwidth, *FOM* is the ADC's figure-of-merit (i.e., measuring the power per sample per effective number of quantization step) and defined as [2]

$$\text{FOM} = \frac{P}{f_s \cdot 2^{\text{ENOB}}} \tag{14}$$

C_1 and C_2 are technology constants[2], and G_A is the amplifier gain [33]. The tunable parameters for the AIC system are N, M, *ENOB*, and the gain G_A, while for the high-speed ADC system they are only *ENOB*, and the gain G_A. Note that the gain G_A is set differently for the AIC system (i.e., in (13)), as compared to the high-speed ADC system (i.e., in (12)). In the high-speed ADC system, the ADC directly samples the input signal, while in the AIC system the ADCs sample the output of the integrator, which is an accumulated signal (see Fig. 2). Since the accumulated signal has larger range than the original signal, the required amplifier gain G_A to accommodate the ADC's input range is potentially much lower in the AIC system than in the high-speed ADC system, for the same application. It should be noted that the required gain G_A depends on the application and the signal of interest.

Beside difference in G_A, the main difference between the power of the AIC system, $P_{\text{AIC,sys}}$, and the high-speed ADC, $P_{\text{ADC,sys}}$, is an extra factor of $(M \cdot N)/(4)$ in the AIC's amplifier power and an extra factor of $(M)/(N)$ in the AIC's ADCs power. The reason for these extra factors is described later in this section. It should also be noted that ADCs, utilized in the AIC system, have much lower *FOM* than a high-speed ADC since they work at much lower frequency. In our evaluation, *FOMs* of 0.5, 1 and 5 pJ/conversion-step are used to represent a range of possible efficiencies for state-of-the-art and future high-speed ADC designs [34] while *FOM* of 100 fJ/conversion-step is used for the AIC system, consistent with the general performance of state-of-the-art moderate-rate ADCs [33].

We now proceed with the derivation of (12) and (13). To do this, we build on our power models previously proposed in [33], with more focus on the noise constraints, as well as emphasizing detailed differences between the power models used in the AIC and the high-speed ADC systems. We then use (12) and (13) to evaluate and compare the energy costs of both systems.

A. High-Speed ADC System Power Model

The total power (12) of the high-speed ADC system, is simply the sum of the ADC power and the amplifier power.

For the ADC, the power can be expressed as:

$$P_{\text{ADC}} = \text{FOM} \cdot 2^{\text{ENOB}} \cdot 2\text{BW}_f \tag{15}$$

where *FOM* is the ADC figure-of-merit, BW_f is signal bandwidth, and *ENOB* equals the ADC's resolution [33].

For the amplifier, the minimum required power is typically determined by the input referred noise $(v_{\text{ni,rms}})$. Using another figure-of-merit, *NEF* (known as the noise efficiency factor), introduced in [35]:

$$\text{NEF} = v_{\text{ni,rms}} \sqrt{\frac{2I_{\text{amp}}}{\pi \cdot V_T \cdot 4k \cdot T \cdot \text{BW}_f}} \tag{16}$$

where I_{amp} is the current drawn by the amplifier, the required power for the amplifier in the high-speed ADC system can then be described by

$$P_{\text{amp}} = V_{\text{DD}} I_{\text{amp}} = V_{\text{DD}} \cdot \frac{\text{NEF}^2}{v_{\text{ni,rms}}^2} \cdot \frac{\pi \cdot V_T \cdot 4k \cdot T \cdot \text{BW}_f}{2}. \tag{17}$$

In addition, here the total output noise of the amplifier needs to be less than the quantization noise of the ADC (see Fig. 3(b))

[2] $C_1 = \pi \cdot V_T \cdot 4kT.\text{NEF}^2/V_{\text{DD}}$, and $C_2 = V_{\text{DD}}^2 \cdot 10\pi \cdot C_p/16$, where V_T is thermal voltage, k is Boltzmann constant, T is absolute temperature, *NEF* is noise efficiency factor of amplifier, V_{DD} is supply voltage, and $\text{C}_p = 6.3$ fF is capacitance at the dominant pole of integrator. $\text{NEF} = 3$ is used which is reasonably conservative [33].

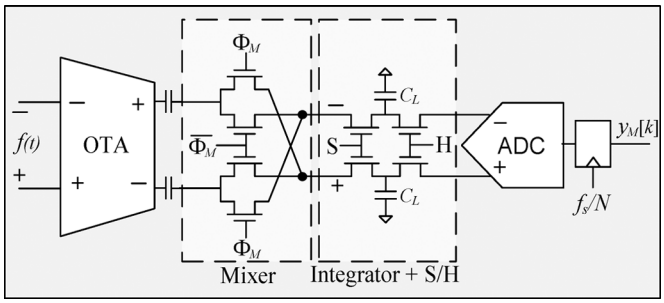

Fig. 13. Circuit block diagram of an AIC branch taken from [33].

which results in the following constraint on the amplifier output noise

$$v_{\mathrm{ni,rms}}^2 \cdot G_A^2 \leq \frac{V_{\mathrm{DD}}^2}{12 \cdot 2^{2\mathrm{ENOB}}} \tag{18}$$

where G_A is the amplifier gain, *ENOB* is the resolution of ADC, and the ADC's input range is equal to V_{DD}.

Using (18) we can obtain a lower bound on the quantity $(1)/(v_{\mathrm{ni,rms}}^2)$, which we substitute into (17) to obtain the minimum power required by the amplifier as

$$P_{\mathrm{amp}} = 2\mathrm{BW}_f \cdot 12 \cdot 2^{2\mathrm{ENOB}} \cdot \frac{G_A^2 \mathrm{NEF}^2}{V_{\mathrm{DD}}} \cdot \pi \cdot V_T \cdot k \cdot T. \tag{19}$$

Hence, using (15) and (19), the total power of the high-speed ADC system, $P_{\mathrm{ADC,sys}}$, equals (12).

B. AIC System Power Model

Fig. 13 shows a detailed block diagram of a single branch of the AIC system (out of M branches). The total power (13) of the AIC system is simply the sum of the ADC power, integrator power, and the amplifier power[3].

For the ADCs power, we account for M ADCs, each sampling at f_s/N

$$P_{\mathrm{ADCs}} = \left(\frac{M}{N}\right) \cdot \mathrm{FOM} \cdot 2^{\mathrm{ENOB}} \cdot 2\mathrm{BW}_f. \tag{20}$$

The integrator power and the power due to switching of the integrator and Sample and Hold (S/H) circuits can be modeled by

$$P_{\mathrm{int}} = M \cdot V_{\mathrm{DD}}^2 \left(\frac{C_L}{16} + C_G\right) \cdot \frac{f_s}{N} \tag{21}$$

where C_L is the integrating capacitor and C_G is the total gate capacitance of the switches where it is negligible compared to C_{L} (see Fig. 13). In addition, it is assumed that the common mode reset is at $0.5\mathrm{V}_{\mathrm{DD}}$ and the voltage swing is $\pm 0.25\mathrm{V}_{\mathrm{DD}}$. As described in [33], the lower bound on the size of the integrating capacitor (C_L) to functionally act as an integrator can be described by

$$C_L > 10\pi \cdot N \cdot C_p \tag{22}$$

[3]The power dissipation of pseudorandom generator is not included since there are ways to significantly reduce the complexity of the matrix generator by using the mixing of PN sequences [33], and in advance technologies; the energy-cost of matrix generator would be negligible compare to other blocks.

where C_p is the capacitance at the dominant pole. Combining (21) and (22), the minimum power required by integrator can be expressed as

$$P_{\mathrm{int}} = 2\mathrm{BW}_f \cdot \frac{M \cdot V_{\mathrm{DD}}^2 \cdot 10\pi \cdot C_p}{16}. \tag{23}$$

For the operational transconductance amplifier (OTA) power in the AIC system, the expression (19) needs to be modified to

$$P_{\mathrm{amp}} = 2\mathrm{BW}_f \cdot 3M \cdot N \cdot 2^{2\mathrm{ENOB}} \cdot \frac{G_A^2 \mathrm{NEF}^2}{V_{\mathrm{DDA}}} \cdot \pi \cdot V_T \cdot k \cdot T \tag{24}$$

where (24) differs from (19) in the appearance of the parameters M and N, and missing a constant factor of 4. With array of M amplifiers in the AIC system

$$\begin{aligned} P_{\mathrm{amp}} &= M \cdot V_{\mathrm{DD}} I_{\mathrm{amp}} \\ &= M \cdot V_{\mathrm{DD}} \cdot \frac{\mathrm{NEF}^2}{v_{\mathrm{ni,rms}}^2} \cdot \frac{\pi \cdot V_T \cdot 4k \cdot T \cdot \mathrm{BW}_f}{2}. \end{aligned} \tag{25}$$

As we will explain later on, the constraint of the output noise will now be

$$v_{\mathrm{ni,rms}}^2 \cdot G_A^2 \cdot N \leq \frac{4V_{\mathrm{DD}}^2}{12 \cdot 2^{2\mathrm{ENOB}}} \tag{26}$$

Finally, using (26) to get a lower bound on the quantity $(1)/(v_{\mathrm{ni,rms}}^2)$, we substitute that lower bound in (25) to obtain (24).

The AIC system requires the total integrated output noise to be less than the quantization noise of the ADC (see Fig. 3(a)). In the AIC system, we are integrating over N samples modulated by a pseudorandom binary sequence (PRBS) and hence the accumulated noise in the output of integrator increases by a factor of $\sqrt{N}$. Since the total output noise must still be kept smaller than the quantization noise, the input referred noise $(v_{\mathrm{ni,rms}})$ needs to be adjusted by a factor of $\sqrt{N}$ to keep the total output noise smaller than the quantization noise. Finally, the reason for an extra factor of 4 in (26) is because the input of the ADC is differential in the AIC system (see Fig. 13). Therefore, the input range of the ADC is $2V_{\mathrm{DD}}$ differentially which accounts for the additional factor of 4.

We next analyze the energy-efficiency of the two systems using our power models (i.e., (12) and (13)).

C. Relative Power Cost of AIC versus High-Speed ADC

The AIC system power, $P_{\mathrm{AIC,sys}}$ (13), is a function of the *ENOB*, M and amplifier gain G_A. As mentioned earlier, the gain G_A needs to be set differently in both AIC and high-speed ADC systems; G_A needs to be set higher in the high-speed ADC system, whereby the relative ratio between the gains depends on application and the signal of interest. For example, in our cognitive radio setup, the relative ratio between G_A gains is about 20. Fig. 14 plots the total power (12) and (13) versus ENOB, for both high-speed ADC and AIC systems, and also for different M in our cognitive radio setup. In Fig. 14(a), we compare system power for relatively small gain scenario (large input signal) where G_A is set to 40 and 2 for the high-speed

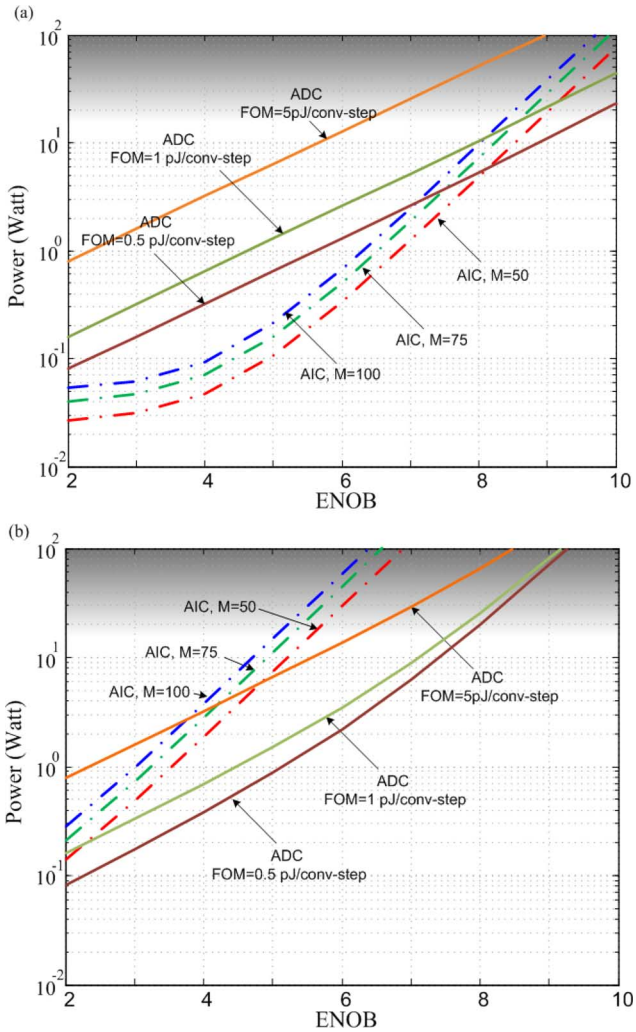

Fig. 14. Power versus required ENOB for applications which require (a) low amplifier gain ($G_A = 40$ in the high-speed ADC system and $G_A = 2$ in the AIC system), and (b) high amplifier gain ($G_A = 400$ in the high-speed ADC system and $G_A = 20$ in the AIC system).

ADC and the AIC system, respectively. In Fig. 14(b) we investigate a higher required gain scenario (small input signal) where G_A is set to 400 and 20, respectively. Note that although the power costs are plotted over a wide range of ENOB, high ENOB values are achievable only when jitter noise and aperture error are very small. As to be expected, when the amplifier gain is low, the AIC power flattens for ENOBs less than 5 since the power is dominated by the integrator power (independent of ENOB). For higher resolutions (i.e., higher ENOB), the amplifier power becomes dominant in the AIC system, since it depends exponentially on ENOB. The main takeaway from Fig. 14 is that at lower gain requirements and low to moderate resolutions (4–6 ENOB, which are also achievable for practical jitter and aperture values), AICs have the potential to be 2–10 $\times$ more power-efficient than high-speed ADCs. Fig. 14 also shows that increasing M increases the AIC power, as the number of components scales upwards with increasing number of measurements. However, increasing M also improves the CS reconstruction, which enables higher ENOB for larger S in the AIC system. Finally, note that the grayed areas in the plots show impractical regions due to chip thermal and power-density limits.

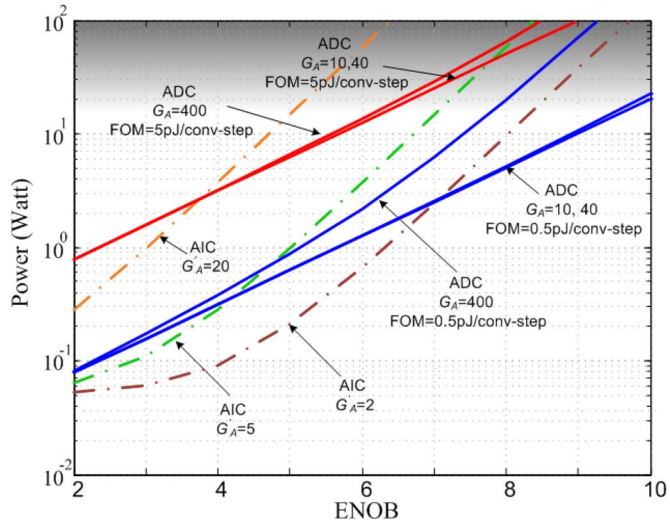

Fig. 15. Power for the required ENOB and different receiver gain requirements, $N = 1000$ and $M = 100$.

To get a sense of potential AIC advantages in other applications, we consider different gains (and also relative ratios between gains) for both AIC and high-speed ADC systems. Fig. 15 shows the power of both systems versus ENOB for different values of gain G_A when $M = 100$. Note that both the systems have different dependence on amplifier gain G_A. For the AIC, the power increases as G_A increases, but on the other hand, the high-speed ADC power changes very little since the power of the single amplifier is not dominant. However, for a high-speed ADC with a very low *FOM*, amplifier power becomes dominant for high ENOB and as a result the high-speed ADC system power increases with G_A. In conclusion, the AIC system has lower power/energy cost and enables roughly 2–10X reduction in power for applications that require low amplifier gain and low to moderate resolution.

VI. Conclusion

In this work, we compare both energy cost and performance limitations of AIC and high-speed ADC systems, in the context of cognitive radio applications where the input signal is sparse in the frequency domain. Our findings report that jitter and aperture effects in the mixing stage of AIC systems limit their resolution and performance. Hence, this contests the proposal that AICs can potentially overcome the resolution and performance limitations of high-speed Nyquist ADCs. We show that currently proposed AIC topologies are sensitive to jitter and aperture errors. We also show that sparse matrices do not improve the resolution performance of AIC. Finally, using realistic power models for both AIC and high-speed ADC systems, we show that AICs have the potential to enable a 2–10X reduction in power for applications where low signal gain and low to moderate resolution are acceptable.

Appendix I

A. Reconstruction Method.

While (8) is a common way to perform CS reconstruction, in this paper we used a different algorithm known as *least angle*

regression (LARS). This is because in our setting, the parameter ε in (8) is not easy to choose since the noise $\boldsymbol{n}^o$ in (7) is non-Gaussian (we cannot simply pick ε proportional to the standard deviation). The LARS algorithm, or more specifically its *least absolute shrinkage and selection operator* (LASSO) modification, is easier to use because of the following. In each iteration, LARS-LASSO produces a LASSO fitted solution that corresponds to some LASSO regularization value. All solutions that it produces in all iterations are generated by the homotopy rule. The LASSO solution in the current iteration is related to the LASSO solution in the previous iteration. It is obtained by slowly changing the previous regularization value until we get a LASSO solution that differs in sparsity by 1. In summary, the LARS algorithm generates all LASSO solutions that are "most spaced-out by sparsity".

So, LARS only requires us to pick which iteration's solution to use, as opposed to picking one value for ε (out of infinite set of possible choices). For every CS reconstruction instance, we pick the iteration using an *oracle* to be as optimistic for AIC as possible. Since we know the actual signal, we simply pick the iteration that gives the smallest error—this is the "best LASSO solution". This oracle uses extra information (the iteration that delivers the smallest error) not known in practice, thus cannot be actually implemented. However, running our experiments this way gives a "lower bound" on the reconstruction error of an actual AIC (one that does not know the signal). Furthermore, this oracle is easy to implement and reproduce, and avoids complicated arguments for tweaking regularization parameters.

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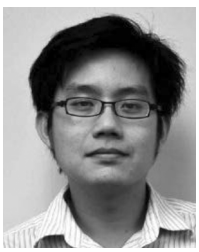
Mr. Abari was the recipient of the Merrill Lynch fellowship in 2011, the Natural Sciences and Engineering Research Council of Canada (NSERC) Postgraduate scholarship, Ontario Professional Engineers Foundation for Education Scholarship and Senate Medal for Outstanding Academic Achievement in 2010.



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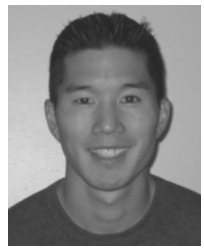

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Prof. Stojanović received the 2006 IBM Faculty Partnership Award, and the 2009 NSF CAREER Award as well as the 2008 ICCAD William J. McCalla, 2008 IEEE Transactions on Advanced Packaging, and 2010 ISSCC Jack Raper best paper awards. He is an IEEE Solid-State Circuits Society Distinguished Lecturer for the 2012–2013 term.