

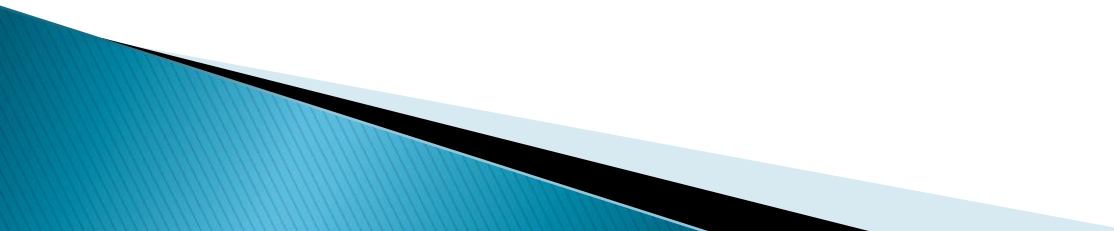
CS 194 Project Checkpoint

Exploring Latency Constraints of Co-Processing Units

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Outline

- ▶ Original Plan
 - ▶ Accomplishments
 - ▶ Problems
 - ▶ Revised Plan
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Original Plan

- ▶ Analyze and Synthesize
 - First quarter: Analysis
 - Develop the test platform.
 - Test the different hardware models.
 - Second quarter: Synthesis
 - From the data, determine that “sweet spot.”
 - Validate the data with real world hardware.

Accomplishments

▶ Vtune Tests

- Dozens of different processor loads recorded.
 - On average, Vtune recommends increasing the number of processors in the computer to a degree of 44.3%
 - Charts in Vtune also show that background processes account for approximately 31.4% of the main memory usage.

▶ Classic PTLsim Tests

- Efficiency of programs in a solitary environment recorded.
 - Instruction count, cycle count, throughput, page faults, cache misses in L1 and L2, branch prediction, and writeback statistics are known.
- Analyzed code and evaluated how to change it so that the desired hardware can be simulated.

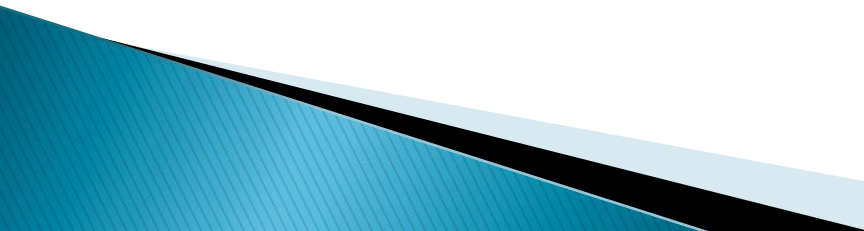
▶ Full Simulation PTLsim/XEN

- Patched kernels to allow for PTLsim enhancements.
- Gained lots of experience in system's administration tasks and operating system's practicals.
- Recently acquired and configured fully compliant hardware.

Problems Faced

- ▶ Hardware Issues
 - SATA Hard Drive failed in test machine.
 - Virtualization technology support is hard to come by.
- ▶ PTLsim/XEN
 - Code is difficult to change.
 - System's work requires tons of time while juggling operating systems.
 - XEN technologies are still fairly new and not well supported.
 - Little help in general with XEN technologies.
 - Nothing works "out-of-the-box"
- ▶ Vtune
 - Reproducibility is sometimes challenging.

Revised Plan

- ▶ Produce working simulation environment under PTLsim/XEN.
 - ▶ Run a wide variety of tests in the simulation environment under different hardware scenarios.
 - The goal is to get at least five different software scenarios tested under at least five different hardware simulations.
 - ▶ Determine the “sweet spot” for a hardware implementation of a co-processing board.
 - Go back and run more tests in Classic PTLsim or Vtune if necessary.
 - ▶ Time permitting, validate “sweet spot” with hardware implementation in real-world co-processing board.
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Summary

- ▶ Original plan did not properly estimate the time it would take to set up the simulation environment.
 - ▶ Data collected can establish the need for more processing power and show isolated program execution.
 - ▶ There's a lot of momentum going into the second quarter but it is questionable whether the tests can be verified.
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