Chapter 4

Exercise 4.1

(a) figure 4.17(a) presents a valid gate network

(b) the network in figure 4.17(b) is not valid since:

- the load factor (L) imposed to one of the 2-input AND gates exceeds the fan-out factor (F) of this gate;
- two outputs are connected together.

(c)figure 4.17(c) presents a valid network.

Exercise 4.3

Gates:

Gate	Type	Inputs	Output
A	AND-2	A_1 A_2	A_3
B	AND-2	B_1 B_2	B_3
C	AND-2	C_1 C_2	C_3
D	OR-2	D_1 D_2	D_3
E	NOT	E_1	E_2

Connections:

FROM	TO
X	A_1
Y	A_2
W	B_1
Z	B_2
A_3	D_1
A_3	C_1
B_3	D_2
B_3	E_1
C_3	R
D_3	C_2
E_2	T

Exercise 4.5

The network for this exercise is presented in Figure **??**.

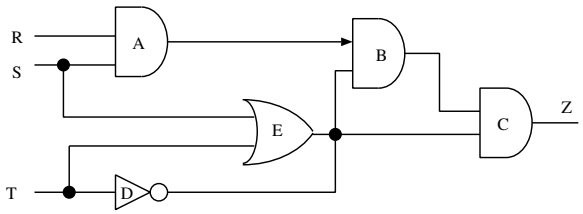

Figure 4.1: Network for Exercise 4.5

It is an invalid network since the outputs of gates D and E are connected to the same point. As we don't know the function implemented by the net, any modification can be done to remove this connection. One possible solution is given in the table that follows:

From	To
R	A_1
S	A_2
A	B_1
B	C_1
E	C_2
T	D_1
A_2	E_1
D_1	E_2
D	B_2
C	Z

Exercise 4.7:
The operation specified by

$$g(x, y, z) = x'yz + xy' + y'z$$

is universal because $g(x, 1, 1) = x'$ realizes the NOT operation, and $g(x, 0, z) = x + z$ realizes the OR operation. Since the set $\{OR, NOT\}$ is universal, the g operation is also universal.

Exercise 4.9

The function * is: $x * y = x'y$. Observe that this function is not commutative ($x * y \neq y * x$). For this reason, the order of inputs must be observed. The NOT gate is obtained as

$$x' = x' \cdot 1 = x * 1$$

The AND gate is mapped to the * function as:

$$x \cdot y = (x')' \cdot y = x' * y = (x * 1) * y$$

The networks to obtain the NOT and AND gates from the "*" gate are shown in Figure **??**. Since the * gate can implement the set {NOT,AND}, and the set {NOT,AND} is universal, the * gate is also universal.

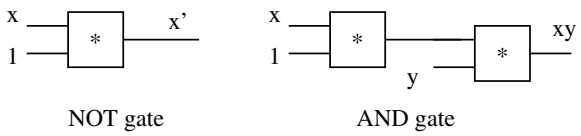

Figure 4.2: Implementing a NOT and AND gates using the * gate

Exercise 4.11

We obtain the following expressions:

$$\begin{aligned} z &= ((x_1' + x_2x_1 + x_1x_0)(x_2x_1 + x_2x_0 + x_2')(x_2x_0 + x_1x_0 + x_0'))' \\ &= ((x_1' + x_2 + x_0)(x_2' + x_1 + x_0)(x_0' + x_1 + x_2))' \\ &= (x_1' + x_2 + x_0)' + (x_2' + x_1 + x_0)' + (x_0' + x_1 + x_2)' \\ &= x_1x_2'x_0' + x_2x_1'x_0' + x_0x_1'x_2' \end{aligned}$$

that is, the output is 1 whenever exactly two of the inputs are 0.

Exercise 4.13

(a)The switching expressions are:

$$\begin{aligned} E_{out} &= E_{in}I_0'I_1'I_2'I_3'I_4'I_5'I_6'I_7' \\ G &= E_{in}E_{out}' \\ z_0 &= E_{in}(I_7 + I_6'I_5 + I_6'I_5'I_4'I_3 + I_6'I_4'I_2'I_1) \\ z_1 &= E_{in}(I_7 + I_6 + I_6'I_5'I_4'I_3 + I_5'I_4'I_2) \\ z_2 &= E_{in}(I_7 + I_6 + I_6'I_5 + I_4) \end{aligned}$$

(b)Since a high-level description is not obvious from these expressions, we evaluate and present the following table:

E_{in}	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	E_{out}	G	z_2	z_1	z_0
0	-	-	-	-	-	-	-	-	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	0	1	0	1	0	0	0
1	0	0	0	0	0	0	1	-	0	1	0	0	1
1	0	0	0	0	0	1	-	-	0	1	0	1	0
1	0	0	0	0	1	-	-	-	0	1	0	1	1
1	0	0	0	1	-	-	-	-	0	1	1	0	0
1	0	0	1	-	-	-	-	-	0	1	1	0	1
1	0	1	-	-	-	-	-	-	0	1	1	1	0
1	1	-	-	-	-	-	-	-	0	1	1	1	1

To get a high-level description we assume that the bit-vector $\underline{z}$ is the radix-2 representation of the integer z. From the table we obtain:

$$z = \begin{cases} j & \text{if } I_j = 1 \text{ and } I_k = 0 \text{ for } k > j \text{ and } E_{in} = 1 \\ 0 & \text{otherwise} \end{cases} \tag{4.1}$$

$$E_{out} = \begin{cases} 1 & \text{if } E_{in} = 1 \text{ and } I_j = 0 \textit{ for all } j \\ 0 & \text{otherwise} \end{cases} \tag{4.2}$$

$$G = \begin{cases} 1 & \text{if } E_{in} = 1 \text{ and } I_j = 1 \textit{ for some } j \\ 0 & \text{otherwise} \end{cases} \tag{4.3}$$

In words, let us call E_{in} the module (network) enable. Then:

- E_{out} is 1 when the module is enabled and all I_i inputs are 0.
- G is 1 if the module is enabled and at least one of the I_i inputs is 1.
- z corresponds to the highest index of the inputs I_i with value 1.

Such a network is called a *priority encoder* (studied in Chapter 9).

(c) The load factor of each input is calculated considering that each AND or NOT gate has an input factor of 1.

Input	Load Factor
E'_{in}	1
I'_7	2
I'_6	2
I'_5	2
I'_4	2
I'_3	2
I'_2	2
I'_1	2
I'_0	1

The maximum delay for the network is obtained considering number and type of gates of each path from inputs to the outputs. The critical path in this case is the one that goes from input I'_6 to output z'_0.

$$T_{pLH}(I'_6, z'_0) = t_{pLH}(\text{NOT}) + t_{pHL}(\text{NOT}) + t_{pHL}(\text{AND-5}) + t_{pHL}(\text{OR-4}) + t_{pLH}(\text{NOT})$$

$$T_{pLH}(I'_6, z'_0) = (0.02 + 0.038 * 2) + (0.05 + 0.017 * 3) + T_1 + (0.45 + 0.025 * 1) + (0.02 + 0.038 * L)$$

$$T_{pLH}(I'_6, z'_0) = 0.692 + T_1 + 0.038 * L$$

$$T_{pHL}(I'_6, z'_0) = t_{pHL}(\text{NOT}) + t_{pLH}(\text{NOT}) + t_{pLH}(\text{AND-5}) + t_{pLH}(\text{OR-4}) + t_{pHL}(\text{NOT})$$

$$T_{pHL}(I'_6, z'_0) = (0.05 + 0.017 * 2) + (0.02 + 0.038 * 3) + T_2 + (0.13 + 0.038 * 1) + (0.05 + 0.017 * L)$$

$$T_{pHL}(I'_6, z'_0) = 0.436 + T_2 + 0.017 * L$$

where T_1 and T_2 are the HL and LH propagation delays for an AND gate with 5 inputs and load factor of 1, respectively. The values of T_1 and T_2 are obtained by decomposition of the AND-5 gate into the gates listed in Table 3.1 of the book. This decomposition is:

$$AND(x_4, x_3, x_2, x_1, x_0) = AND(AND(x_4, x_3, x_2), AND(x_1, x_0))$$

The resulting delays are:

$$\begin{aligned} T_1 &= t_{pHL}(\text{AND-3}) + t_{pHL}(\text{AND-2}) = 0.18 + 0.018 + 0.16 + 0.017L = 0.358 + 0.017L = 0.392 \\ T_2 &= t_{pLH}(\text{AND-3}) + t_{pLH}(\text{AND-2}) = 0.2 + 0.038 + 0.15 + 0.037L = 0.388 + 0.037L = 0.462 \end{aligned}$$

The delays of the critical path become:

$$T_{pHL}(I'_6, z'_0) = 0.436 + 0.462 + 0.017L = 0.90 + 0.017L$$

$$T_{pLH}(I'_6, z'_0) = 0.692 + 0.392 + 0.038L = 1.08 + 0.038L$$

(d) Timing diagram, see figure **??**:

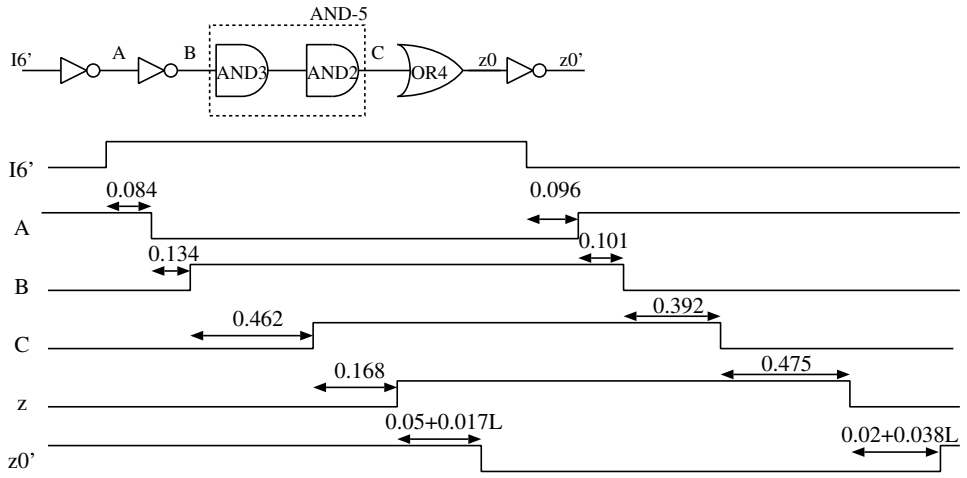

Figure 4.3: Timing diagram of Exercise 4.13

Exercise 4.15

We define the modules as indicated in figure **??**. For module M_1 we obtain the switching expression:

$$y = (abc + ab'c' + a'bc' + a'b'c)'$$

A high-level description is:

$$y = \begin{cases} 1 & \text{if there are 0 or 2 inputs with value 1} \\ 0 & \text{otherwise} \end{cases} \tag{4.4}$$

Module M_1 implements a 3-input even-parity function which we denote $EP(a, b, c)$.

Module M_2 has three inputs e, f and g, and two outputs z_1 and z_0. The switching expressions are:

$$z_1 = (efg + ef'g' + e'fg' + e'f'g)'$$

$$z_0 = (e'f'g' + e'fg + ef'g + efg')'$$

The first expression corresponds to the even-parity function $EP(e, f, g)$ and the second one to the odd-parity function $OP(e, f, g)$.

By substitution we obtain:

$$z_1 = EP(EP(I_8, I_7, I_6), EP(I_5, I_4, I_3), EP(I_2, I_1, I_0)) = OP(I_8, I_7, ..., I_0)$$

since an even number of groups (among 3 groups) with an even number of 1 inputs correspond to an odd number of 1 inputs overall.

$$z_0 = OP(EP(I_8, I_7, I_6), EP(I_5, I_4, I_3), EP(I_2, I_1, I_0)) = EP(I_8, I_7, ..., I_0)$$

since an odd number of groups (among 3 groups) with an even number of 1 inputs correspond to an even number of 1 inputs overall.

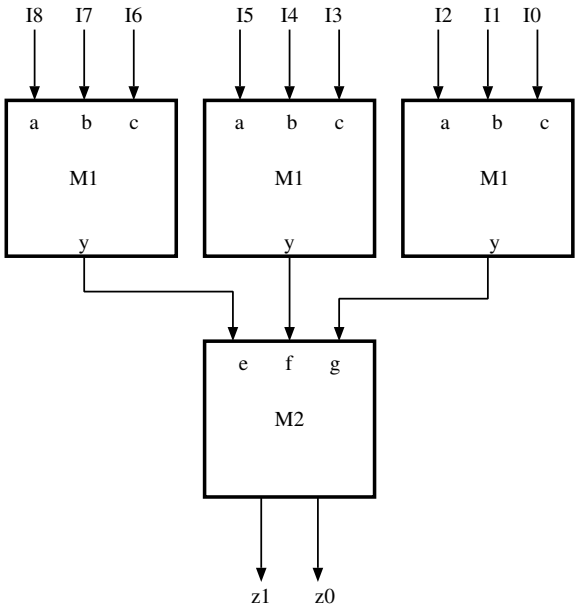

Figure 4.4: Modules used in Exercise 4.15

That is, the network implements the even-parity and odd-parity functions of nine inputs.

Delay of the network is obtained by the following expression for the path from input I_2 to output z_1:

$$\begin{aligned} T_{pLH}(I_2 - z_1) &= t_{pLH}(NOT) + t_{pHL}(\text{OR-4}) + t_{pHL}(\text{AND-3}) + t_{pHL}(\text{NOT}) + \\ &\quad t_{pLH}(\text{NOT}) + t_{pHL}(\text{OR-4}) + t_{pHL}(\text{AND-3}) + t_{pHL}(\text{NOT}) + t_{pLH}(\text{NOT}) \\ &= 0.02 + 0.038L + 0.45 + 0.025 \times 1 + 0.18 + 0.018 \times 1 + 0.05 + 0.017 \times 4 + \\ &\quad 0.02 + 0.038 \times 5 + 0.45 + 0.025 \times 1 + 0.18 + 0.018 \times 1 + 0.05 + 0.017 \times 2 + \\ &\quad 0.02 + 0.038 \times 3 \\ &= 1.91 + 0.038L \end{aligned}$$

$$\begin{aligned} T_{pHL}(I_2 - z_1) &= t_{pHL}(NOT) + t_{pLH}(\text{OR-4}) + t_{pLH}(\text{AND-3}) + t_{pLH}(\text{NOT}) + \\ &\quad t_{pHL}(\text{NOT}) + t_{pLH}(\text{OR-4}) + t_{pLH}(\text{AND-3}) + t_{pLH}(\text{NOT}) + t_{pHL}(\text{NOT}) \\ &= 0.05 + 0.017L + 0.13 + 0.038 \times 1 + 0.2 + 0.038 \times 1 + 0.02 + 0.038 \times 4 + \\ &\quad 0.05 + 0.017 \times 5 + 0.13 + 0.038 \times 1 + 0.2 + 0.038 \times 1 + 0.02 + 0.038 \times 2 + \\ &\quad 0.05 + 0.017 \times 3 \\ &= 1.37 + 0.017L \end{aligned}$$