Sensor Network Architecture

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1. OVERVIEW

Emergence of the concept of multihop ad-hoc wireless networks, low power electronics, low power short-range wireless communication radios, and intelligent sensors are considered as the major technological enablers for the deployment of sensor networks (SNs). Our goal in this survey is to identify the key architectural and design issues related to sensor networks, critically evaluate the proposed solutions, and outline the most challenging research directions. The evaluation has three levels of abstraction: individual components on SN nodes (processor, communication, storage, sensors and/or actuators, and power supply), node level, and distributed networked system level. Special emphasis is placed on architecture, system software, and on challenges related to the usage of new types of components in networked systems. The evaluation process is guided by the anticipated technology trends, the current and the future applications. The main conclusion of the analysis is that the architectural and synthesis emphasis will be shifted from computation and communication components to sensors and actuators, and different types of sensors and applications that require distinctly different architectures at all three levels of abstraction.

2. MOTIVATION AND OBJECTIVES

Embedded wireless sensor networks (SNs) are systems consisting of a large number of nodes each equipped with certain amount of computational, communication, storage, sensing, and often actuation resources [Est99]. SNs aim to provide an efficient and effective connection between the physical and computational worlds. Therefore, SNs are widely considered as the new frontier for the Internet. Furthermore, they may potentially have high economic impact in many fields including military, education, monitoring, retail, and science. At the same time, SNs propose numerous new research and development challenges, including the need for the next generation low power, low cost, small size, error and fault resiliency, flexibility, conceptually new security and privacy mechanisms, and new types of input/output (I/O) operations. However, before any of these challenges can be properly addressed the sensor network must be in place: the network has to be designed and implemented, and there has to exist flexible mechanisms and the means for their efficient and convenient use. In addition to algorithms, hardware and software architecture will significantly impact the effectiveness of SNs. Furthermore, SN design methodologies will have an important impact on the cost and performance of SNs. The third aspect with a major potential impact is the modeling techniques for SN, but they are out of the scope of this survey. Comprehensive surveys on sensor networks include [Est99, Pot00, Aky02].

Our overall strategic goal is to summarize what is currently the state-of-the-art with respect to architecture and synthesis techniques for sensor networks and to provide a starting point and impetus for research and development of new architectures and synthesis tools for sensor networks. More specifically, the emphasis is on:

* *Identifying Requirements for Typical SN Application.* Traditionally, design of new computer architectures have been based on comprehensive and representative benchmarks suites for typical target applications. It is of exceptional importance to create such benchmarks for sensor networks. In addition, it is important to predict the nature of future SN applications. However, even before the benchmarks are available, qualitative analysis of representative application can greatly facilitate identification of more accurate design goals.

* *Identifying Relevant Technological Trends.* It is well known that many electronics and optical systems follow exponential performance growth rates. SN systems are heterogeneous and complex, therefore it is important to anticipate which design and cost bottlenecks are intrinsic, and which ones will be resolved due to technological progress. Importance of technological trends is well illustrated during power optimization. Depending on future ratios of computation, communication and storage cost, very different types of algorithms will be best suited for SNs.

* *Balanced Design.* In order to achieve a balanced design, the first instinct could be to optimize each and every component to the maximal extent. From research and economic point of view, it is important to identify where to focus the main optimization effort. In addition, new computational models are needed, but one has to keep in mind that they are not the ultimate goal per se.

* *Techniques for Design and the usage of the Design Components.* The six components of SN node can be grouped in two categories according to their maturity. Power supplies, in particular, storage and power supply, are considered as mature technologies. On the other hand, ultra low power wireless communication, sensors, and actuators are technologies waiting for major technological revolutions. It is important to identify which techniques, architectures, and tools can be reused and where the new design effort is required.

* *Overall Node Architecture and Trade-offs*. One can envision a number of possible trade-offs. For example, TinyOS approach [Hil00] advocates aggressive communication strategy in order to reduce complexity of computation and storage at local sensor nodes. On the other hand, sensor-centered approach [Fen02] advocates aggressive sensor data processing, filtering, and compression in order to reduce communication.

* *Survey of the state-of-the-art technology, components, sensor network nodes*. Special emphasis is placed on providing both qualitatively and quantitative analysis. In addition, we survey several state-of-the-art sensor nodes and critically evaluate decision that influenced their structure.

3. SNs – GLOBAL VIEW AND REQUIREMENTS

It is well known that characteristics of computing or communication systems are direct consequences of targeted applications. We have identified a number of characteristics of sensor networks that have direct impact on architectural and design decisions. These characteristics rise naturally from confluence of typical application requirements and technology limitations. Typical SN applications include contaminant transport monitoring, marine microorganisms analysis, habitat sensing, and seismic and home monitoring [Cer01]. These applications show a great deal of diversity. Nevertheless, a number of general characteristics are shared among the majority of SN applications regardless of the specific types of sensors and application objectives. These characteristics include low cost, small size, low power consumption, robustness, flexibility, resiliency on errors and faults, autonomous mode of operation, and often privacy and security.

Sensor network nodes typically consist of six components: processor, radio, local storage, sensors and/or actuators, and power supply. There are a number of relevant technology trends that have to be considered for example, a huge variety of powerful low-power, low-cost processors, and low-cost memory technologies are wildly accessible. Also, both memory and processor are growing more and more powerful according to Moore's Law, and wireless bandwidth has increased by a factor of more than hundred in the last seven years yet, the capacity of batteries is only growing at a rate as low as 3% per year. The cost of application-specific designs is growing rapidly: the cost of

masks alone is one million dollars and keep increasing by the factor of two every two years. Sensors and actuators are relatively young industrial fields and predictions are still uncertain.

Due to these application requirements and technology constraints, we believe that the following architectural and design objectives are most relevant:

* *Small physical size.* Reducing physical size has always been one of the key design issues. Therefore, the goal is to provide powerful processor, memory, radio and other components while keeping a reasonably small size, dictated by a specific application.

* *Low power consumption.* The capability, lifetime, and performance of the sensors are all constrained by energy. The sensors have to be active for a reasonable long period of time without recharging the battery, because maintenance is expensive.

* *Concurrency-intensive operation.* In order to achieve the best overall performance, the sensor data has to be captured from the sensor, processed, compressed, and then sent to the network simultaneously in a pipelined processing mode, instead of sequential action. There are two conceptual approaches to address this requirement: (i) partitioning the processor into multiple units where each is assigned to a specific task; and (ii) reduction of the context switching time.

* *Diversity in design and usage.* Since we want each node to be small in size, low on power consumption, and have limited physical parallelism, the sensor nodes tend to be application specific. However, different sensors have different requirements for example, cameras and simple thermometers are two extremes in terms of the functionality and complexity. Therefore, the design should facilitate the trade-offs between reuse, cost, and efficiency.

* *Robust Operations.* Since the sensors are going to be deployed over a large and sometimes hostile environment [forests, military usage, human body], we expect the sensors to be fault and error tolerant. Therefore, sensor nodes need the ability to self-test, self-calibrate, and self-repair [Kou02].

* *Security and Privacy.* Each sensor node should have sufficient security mechanisms in order to prevent unauthorized access, attacks, and unintentional damage of the information inside of the SN node. Furthermore, additional privacy mechanisms must also be included.

* *Compatibility*. The cost to develop software dominates the cost of the overall system. In particular, it is important to be able to reuse the legacy code through binary compatibility or binary translation.

* *Flexibility*. There is a need to accommodate functional and timing changes. Flexibility can be achieved through two means: (i) programmability - by employing programmable processors such as microprocessors, DSP processors and microcontrollers; and (ii) reconfiguration by using FPGA-based platforms. We envision that flexibility will be mainly achieved by programmability and use of specialized ASIC and co-processors due to low power consumption.

4. INDIVIDUAL COMPONENTS OF SN NODES

SN nodes generally are composed of the following six components: processor, storage unit, power supply, sensors and/or actuators, and finally communication (radio) subsystems. It is apparent that standard processor, possibly augmented with DSP and other co-processors and some ASIC units will provide adequate processing capabilities at acceptably low energy rates. Also note that the state-of-the-art of the actuators is such that they are still not used in the current generation of SN nodes. Therefore, we focus our attention on the other five components. For the sake of completeness, we will start by presenting a processor that is specifically designed for sensor networks.

4.1 PROCESSOR

Berkeley BWRC research group designed and implemented a prototype processor. The main target areas of the processor include voice processing and related applications for wireless devices. For example, the processor can be used in museums to provide better interaction between visitors and displayed items. The Maia processor [Zha00] is build around an ARM8 core with 21 co-processors. These 21 processors include: two MACs, two ALUs, eight address generators, eight embedded memories, and an embedded low-energy FPGA [Geo99]. The goal is to provide

enough parallelism at low energy levels. ARM8 core configures the memory-mapped satellites using a 32 bit configurable bus and also communicates data with the satellite co-processors using 2 pairs of I/O interface ports by applying direct memory reads/writes. The interactions between the ARM8 and the co-processor satellites are carried out through an interface control unit. A 2-level hierarchical mesh-structured reconfigurable interconnect network is used to establish the connections between all satellites. This network provides a favorable trade-off between bandwidth and low area (cost) and low power requirements. This 210-pin chip contains 1.2M transistors and measures 5.2x6.7mm^2 in 0.25µm 6-metal CMOS. In order to minimize the overall energy consumption, the embedded ARM8 core is additionally optimized and can operate under variable supply voltages [Bur00]. In addition, both the dualstage pipelined MAC and the ALU are configurable. The address generators and embedded memories provide multiple concurrent data streams to the computational components. The embedded FPGA has a 4x8 array of 5-input 3-output CLBs. It can be optimized for tasks such as arithmetic operations and data-flow control functions. The interface control unit interacts and coordinates the synchronization and communication between the synchronous ARM8 core and the asynchronous reconfigurable datapaths. It also enables the ARM8 core to reconfigure the satellites. The overall targeted computation model is globally-asynchronous locally-synchronous computations and supports multi-rate operation.

4.2 STORAGE

Depending on the overall sensor network structure, the requirements for storage in terms of fast and nonvolatile memory at each node can be sharply different. For example, if one follows the architecture model where all information is instantaneously sent to the central node, there is very little need for local storage on individual nodes. However, in a more likely scenario, where the goal is to minimize the amount of communication and conduct significant part of computation at each individual node, there will be significant requirement for local storage. There are at least two alternatives for storing data in a local node.

The first option is to use flash memory. Flash memory is very attractive in terms of cost and storage capacity. However, it has relatively severe limitations in terms of how many times it could be used for storing different data in same physical locations [Ish01]. The second option is to use nano-electronics based MRAM [Sla02]. It is expected that MRAM will soon be able to support significant number of applications in a number of areas.

It is important to note that historically both non-volatile semiconductor and disk storage capacity have been growing at the rate that is higher than the Moore's law. We envision at least two major challenges for the use of non-volatile memory in sensor nodes: partitioning for power reduction and developing memory structures that will fit the short word-lengths of data produced by sensors. Note that significant percentage of both network control and sensor data will have low entropy. Therefore, it is likely that aggressive compression techniques will be used to reduce amount of data that has to be stored or transferred [Dri03]. In addition, in the case where the node is physically larger, one can store the data in micro disks [Die00].

4.3 POWER SUPPLY

There is a wide consensus that energy will be one of the main technological constraints for SN nodes. For example, the current generation of smart badges and Motes enable continuous operations for only a few hours. There are at least two conceptually different ways that energy supply can be addressed. The first is to equip each sensor node with a (rechargeable) source of energy. There exist two main options for this approach. Currently, the dominant option is to use high-density battery cells [Ful94] [Lin95]. The other alternative is to use full cells [Fir01]. Full cells provide exceptional high density and clean source of energy. However, currently they are not available in physical format that are appropriate for SN nodes.

The second conceptual alternative is harvesting energy available in the environment [Rab00]. In addition to solar cells, which are already widely used for mobile appliances such as calculators, there are a number of proposals for converting vibration to electric energy [Men01]. An interesting solution for power source is introduced in [Dou03]– a batteryless wireless system harvests ambient heat that is used instead of traditional batteries as a power source. The main component of the system is switched-capacitor DC-DC converter and a microthermodelectric module that makes such a system possible. The chip is fabricated in a 0.8m fully depleted SOI process and its effectiveness demonstrated.

4.4 SENSORS

The importance of sensors cannot be overstated. The purpose of sensor network nodes are neither computing, nor communicating, but rather sensing. The sensing component of SN nodes is the current technology bottleneck. The sensing technologies currently are not progressing as fast as semiconductors. There are also conceptual limitations that are significantly stricter for sensors than for processors or storage. For example, sensors interface to the real physical world, while the computing and communicating units are dealing with a greatly controlled environment of a single chip. Transducers are front-end components in sensor nodes that are being used to transform one form of energy into another. Design of transducers is considered out of scope of system architect. In addition, sensors may have four other components: analog, A/D, digital, and micro-controller. The simplest design option includes only the transducer itself. However, the current trend is to put more and more "smartness" into sensor network nodes. Therefore, a significant processing and computing abilities are beingadded to sensor nodes [Mas98].

One of the main challenges of SN that we envision is selecting the type and the quantity of sensors and determine their placement. This task is difficult because there are numerous types of sensors with different properties such as resolution, cost, accuracy, size, and power consumption. In addition, often more than one sensor type is needed to ensure the correctness of operation and that data from different sensor can be combined. For example, in the Cricket Compass [Nis01], the orientation and the movement of the studying object can be obtained by measuring the distance between several fixed-location referencing sensors, therefore the location of sensor is crucial to minimize error [Nis01].

Another challenge is to select the correct type of sensors and the way to operate them. The source of difficulty is sensor interactions. For example, consider determining the distance using audio sensors. Since the speed of the sound depends greatly on both temperature and humidity of the environment, it is necessary to take both measurements into count in order to get the accurate distance.

There are also several other design tasks associated with sensors, including fault tolerance, error control, calibration, and time synchronization [Kou02]. There are a large number of different sensor technologies [IEEEPro03]. As an example, we consider [Kul03, Luo03]. Accelerometer is one of the most popular MEMSbased sensors. A state-of-the-art capacitive accelerometer is recently reported by the MEMS group at the University of Michigan. It uses two-

element sensor array in two S? (sigma-delta) loops to improve accuracy by a factor more than two times in comparison with traditional 2nd order S? modulator. The design is clocked at 1MHz and provides 1V/pF sensitivity. It has dynamic range of more than 120dB and consumes less than 12mW. Another state-of-the-art accelerometer is designed at Carnegie Mellon University. The design combines lateral accelerometer and vertical gyroscopes with signal processing circuits.

4.5 RADIO

Short range radios are exceptionally important as the communication components because the energy dedicated to sending and receiving messages usually dominates the overall energy budget [Rab00]. During the design and the selection of radios, one has to consider at least three different abstraction layers: physical, media access control (MAC), and network. The physical layer is responsible for establishing physical links between a transceiver and one or more receivers. The main tasks at this level involve signal modulation and encoding of data in order to maintain communication in presence of channel noise and signal interferences. In order to efficiently use the bandwidth and reduce the development cost, the standard practice is that several radios share the same interconnect medium. The sharing of media (e.g. time or frequency) is facilitated by the media access control (MAC) layer. Finally, the network layer is responsible for establishing the path that a message has to travel through the network in order to be transferred from its source to the destination.

Design of power and bandwidth efficient radios is one of the main research and development tasks. It is important to realize that the radio architecture is a function of the employed network structure and protocols. The main tradeoff is between the relative energy cost of transmission and reception. The key observation is that listening to the channel is expensive. Therefore, there is a need to develop schemes that will enable long period of sleep mode for receivers. For example, one option is to use coordinated policy for deciding which node will go to sleep while the connectivity in the node is maintained [Roz01]. The other option is to use two radios. One of them is responsible for data reception and is power hungry. It is used only when the other ultra low power radio invokes it. The ultra low power radio is only used to detect if one wants to transmit data to this node.

Table 1 surveys the state-of-the-art radio design alternatives from ISSCC 2001 [ISS01] and ISSCC 2002 [ISS02]. We briefly outline several notable radio designs. One radio design alternative is the fully integrated GPS radio described in [Beh02]. The Low-IF architecture of the radio simultaneously enables a high level of integration and low power consumption. The integrated radio measures a 9.5 mm^2 chip area. It can operate under a various range of voltage and temperature, namely from 2.2 to 3.6V and from - 40°C to + 85°C and consumes 27mW from a 2.2V supply.

Another notable design is the IEEE 802.11a wireless LAN transceivers presented in [Zar02]. A 0.25m CMOS technology is used to integrate a 5GHz transceiver compressing the RF and analog circuits of an IEEE 802.11a-compliant WLAN. The integrated circuit has 22dBm maximum transmitted power, 8dB overall receive-chain noise figure, and –112dBc/Hz synthesizer phase noise at 1 MHz frequency offset.

Other state-of-the-art radio designs include [Chi03, Klu03, Bou03, Cho03]. [Chi03] introduces a fully integrated 2.4GHz transceiver in 0.25m CMOS and its associated baseband processor in 0.15m CMOS. In [Klu03], advanced microdevices has recently designed 2.4GHz CMOS radio for 802.11b wireless LAN. They use 0.25m feature size to design 10mm^2 integrated circuits that consume 86mA in receiver mode and 73mA in transceiver mode from 2.5V supply. The receiver has a short settling time and is equipped with separate receiver channel filter and transceiver pulse shaping filter. In addition, it provides filter calibration circuitry. [Bou03] introduces a digitally calibrated transceiver in 0.18m CMOS that occupies 18.5mm^2. The integrated phase noise can be minimized to less than –37.4dBc using the fully integrated VCO and synthesizer. [Cho03] has developed a 2.4GHz radio for 802.15.4 WPANs using 0.18m CMOS technology that consumes 21mW and 30mW at 1.8V supply in receiving and transmitting mode respectively. It incorporates a poly-phase filter and applies transistor linearization technique to achieve a low-IF architecture. Other alternatives also include [Dar03, Coj03].

5. SENSOR NETWORK NODE

In this section, we address the key issues related to the architecture and synthesis of an individual SN node. Architectural aspects are discussed along three lines: hardware, software, and middleware. While design issues are presented from synthesis and analysis points of view.

There have been at least three main approaches in which the architecture of SN nodes has been addressed [Reconsider wording]. The first group of initial efforts is a number of designs of individual sensor nodes and badges [Agr99, Asa98, Loc02, Mag98, Men01, Pot00, Wan92]. The emphasis of this class is ensuring the creation of working prototypes and, in some cases, pushing the state-of-the-art of an individual component (e.g. radio, low power, energy harvesting). The second group was represented by the Mote/TinyOS development team at UC Berkeley [Cul01, Hil00]. They made the first effort to address the trade-offs between various components of the node by developing new architectures and operating systems (OS). The main characteristic of the last group of efforts is sensor centered. The emphasis is to exploit relatively inexpensive off-the-shelf components in terms of cost and energy as a basis to explore qualitative and quantitative trade-offs between node components and in particularly sensors.

It is difficult to anticipate technological trends, but one can easily identify at least some high impact trends and required solutions. For example, it is apparent that there is a need for overall energy consumption balanced architectures. Another high impact research topic is sensor organization and development of the interface between components. Finally, due to privacy, security and authentication needs, techniques such as unique ID for CPU and other components that facilitate privacy will be in high demand. In the software domain, the main emphasis will be on RTOS (Real Time Operating System) [Li97]. There is a need for ultra aggressive low power management due to energy constraints and a need for comprehensive resource accounting due to demands for privacy and security. In a number of cases support for mobility functions (e.g. location discovery) are also needed. Middleware will be in even stronger demand in order to enable rapid development and deployment of new applications. Tasks such as sensor data filtering, compression, sensor data fusion, sensor data searching and profiling, exposure coverage and tracking will be ubiquitous.

Synthesis of sensor nodes will pose a number of new problems in the CAD world. It is obvious that new types of models, abstractions, and tasks will be defined and solved. For example, sensor allocation and selection, sensor positioning, sensor assignment, and efficient techniques for sensor data storage are typical examples of pending synthesis tasks. Development of conceptually simple, clean, and inexpressive models of computation is of prime

importance as a starting point for synthesis of modern computing systems. The sensor nodes will require not just new models of computations, but also new models of the physical world. One such example is standard Euclidian space with classical physical laws (e.g. Newton's law, Thermodynamics law).

It is well known that parts that are responsible for modern design flow, debugging and verification are the most expensive and time consuming components. Due to the heterogeneous nature and the complex interactions between components, we expect the same in the case of sensor nodes. In particular, we anticipate that the techniques for error and fault discovery, testing, and calibration will be of prime importance. In the rest of this section, we describe four representative SN nodes designs: Berkeley Mote, Piconode nodes, UCLA Medusa II and light compass node.

5.1 BERKELEY MOTE NODE

The starting point for designing modern computer systems is a comprehensive set of benchmarks that are representative for common users. Unfortunately, such a set of benchmarks is not currently available to designers of SN nodes. The starting point for designing Mote wireless sensor network nodes was the set of qualitative observations about the requirements of wireless sensor networks. Special emphasis is placed on small physical size and low energy consumption. In addition, attempts have been made to facilitate concurrency intensive operations, in order to provide control hierarchy and take advantage of the limited physical parallelism. Furthermore, the design decisions are driven by retargetability for robust operations at least at the network level. The design went though several iterations and, until recently, was leveraging on the availability of standard off-the-shelf components. Generally speaking, the design is radio centric in the sense all main decisions are made is such a way to facilitate low energy communications. The main processor is Atmel 90LS8535 microcontroller that has 8-bit Harvard architecture with 16 bit addresses. It achieves speed of 4MHz at 3W. The system has rather minimal amount of memory that consists of 8 Kbytes of flash for program memory and 512 bytes SRAM for data memory. Therefore, the system can be integrated only with low frequency sampling sensors and it has to communicate frequently. The processor integrates a system of timers and counters and can be placed in four energy modes: active, idle, power down, and power save. In the idle mode, the processor is completely shut off. In the power down mode, only the watchdog and asynchronous interrupt logic is awake. Finally in the power save mode, the asynchronous timer is also active in addition to the watchdog and interrupt logic. The system also has co-processor Atmel 90LS2343

microcontroller that has 2 Kbytes flash instruction memory and 128 bytes of SRAM and EEPROM memory. The co-processor can be used to reprogram the main microcontroller.

The authors consider the RF Monolithic 916.50 transceiver as the central part of the design. The radio is equipped with antenna and a system of discrete components that can be used to alter characteristics of the physical layer such as signal strength. The radio operates at speed of 19.2 Kbytes/sec. The transceiver can operate in three modes: transmission, reception and power off. The system can have up to 8 sensors. Two most widely used are photoelectric optical sensor and temperature sensor. Each sensor is placed on the bus that is controlled using software.

It is instructive to consider the power characteristics of the design. The MCU core consumes between 2.5 to 6.5mA. The radio consumes between 5 to 12mA. The optical sensor and temperature sensor consume 0.3 to 1mA respectively. The coprocessor consumes 1 to 2.4mA. Finally, EEPROM consumes 1 to 3mA. In particular, it is instructive to compare energy spent for bit transmission and bit processing. The system spends about 1mJ to send and 0.5mJ to receive 1 bit. At the same time, the system can execute approximately 120 instructions for each mJ spent. The system does not have provision for energy reduction using variable voltage, therefore energy is saved mainly by turning the system off. The core of the system software for the design is an exceptionally compact microthreading operating system (TinyOS). The Berkeley design team concluded that new application domain required a new operating system, therefore they decided not to adopt any of a great variety of RTOS 8 bit controllers. While this decision certainly resulted in higher power efficiency and more interesting system software architecture, it also created additional demands and constraints in programming already highly constrained hardware. Nevertheless, the system has been highly popular in research community. Several thousands copies of various versions of the mote have been used by more than 200 research teams. The greatest strength in the system is its small size and low power. Probably the most serious disadvantages are related to the development of real applications. While motes have been tremendously popular in research community, it is still unclear how well they are suited for applications where more complex systems of sensors are needed.

5.2 UCLA MEDUSA MK-2 NODE

The Medusa MK-2 node is representative of the state-of-the-art design of more powerful sensor nodes [Sav02]. The computational unit of Medusa MK-2 nodes consists of two microcontrollers. The first one is a 8-bit Atmel STMega128L MCU with 4MHz that has 32K of flash memory and 4KB of RAM. This processor serves as an interface between sensors and radio baseband processing. The second microcontroller is an ATMEL ARM THUMB processor enclosed within 120-ball BGA package. It has significantly more processing power at 40MHz. It also includes 136KB of RAM and 1MB of on-chip FLASH memory.

The communication unit of Medusa MK-2 nodes is a combination of a TR 1000 low power radio from RF Monolithics for wireless and a RS-485 serial bus transceiver for wireline communication. The sensing unit has two components: a MEMS accelerometer and a temperature sensor. It can be also augmented with other types of sensors. Medusa nodes also incorporated a variety of interfaces, including 8 10-bit ADC inputs, serial ports and numerous general purpose I/O ports. An ultrasonic ranging unit is implemented on an accessory board that uses 40KHz transducers. Ultrasonic measurements are coordinated with RF measurements in order to calculate inter-node distances and therefore enable localization of nodes. Localization is conducted using iterative linearized multilateration.

The nodes also have two external connectors. The first one is used to communicate with a PC to download and debug software. It also provides the necessary wiring requirements for connecting to an external GPS module. The second connector has a set of ADC and GPIO, and serves as an expansion slot for attaching add-on boards carrying different sensors. Finally, Medusa nodes also have two pushbuttons that serve as a user interface. They are mainlyused for triggering events and executing different tests during experimentations.

It is interesting to take a closer look at the computational unit of Medusa Mk-2 nodes. According to the computation requirements, the computational tasks are classified into two board categories: low demand tasks and high demand low frequency processes. Low demanding tasks are the periodic processes such as baseband processing for the radio while listening for new packets, sensor samplings, handling of sensor events, and power management. Even though these tasks do usually require a high concurrency, they are not particularly demanding in terms of computational

resource requirements and therefore can be easily handled by an 8-bit microcontroller. The Medusa-MK-2 nodes use a low power AVRMega128L microcontroller.

The second category of low frequency high demanding tasks is related to the processing of acquired sensor data in order to produce user requested information. For example, in the case of the fine-grained localization problem, a sensor node is expected to compute an estimate of its own location based on a set of distance measurements to known beacons or neighbors. In order to avoid error propagation, a node has to perform a set of high precision operations. If an 8-bit processor is used to conduct this type of computations, it would result in high latencies and lower precision. Therefore a high-end processor is a more adequate solution. More specifically, Medusa adopts the 40MHz ARM THUMB processor to perform this type of operations. Another advantage is that the node can use existing standard applications and libraries. The THUMB microcontroller also has sufficient resources to support off the shelf embedded operating systems such as Red Hat, eCos, and uCLinux. The inclusion of the THUMB processor is also justified by a comparison of the two processors made from a power/latency perspective conducted by the UCLA group. The THUMB processor executes instructions at the rate of 0.9MIPS per MHz at 40Mhz while consuming 25mA with a 3V supply, which has a performance of 480 MIPS/Watt. On the other hand, the ATMega128L only provides 242 MIPS/Watt performance when operating at 4MHz and consumes 5mA at 3V supply.

Communication between the two processors is handled by a pair of interrupt lines, one for each microcontroller, and a SPI bus. The two nodes remain in sleep mode until an interrupt indicating the need for data exchange occurs. The communication takes place over the 1Mbs SPI bus.

Medusa MK-2 nodes are capable of two types of communications: wired and wireless. All nodes are equipped with both a wired link and a wireless link. The wireless link is a low power TR1000 radio from RF Monolithics. This radio has a maximum transmitting power of 0.75mW and has an approximate transmission range of 20 meters. Two modulation schemes are supported by this radio: On-Off Keying (OOK) and Amplitude Shift Keying (ASK). Selection of the appropriate modulation can be done in software. On a Medusa MK-2 node, the baseband processing for the radio is done by ATMega128L microcontroller. This also allows the node to run the low power S-MAC

[Ye02] protocol on the ATMega128L processor. In addition to the wireless link, Medusa nodes also incorporate an RS-485 serial bus interface for wireline communication. By attaching a low power RS-485 transceiver to one of the RS-232 ports of the THUMB processor, it allows the node to connect to an RS-485 network using an RJ-11 connector and regular telephone wire. A single RS-485 has occupancy up to 32 nodes that span over a total wire length distance of 1000 feet.

The power unit of Medusa MK-2 nodes consists of two main components: the power supply and the Power Management and Tracking Unit PMTU [Che02]. The power supply consists of a 540mAh lithium-ion rechargeable battery and an up-down DC-DC converter that has a 3.3V output that can reach [Generate?] up to 300mA of current from the battery. The power supply is designed in such a way that power-additional sensors can be attached later on as accessory boards, since the node only requires less than 50mA with no sensors attached. By putting the ARM THUMB processor together with the RS-485 and RS-232 transceivers in sleep mode most of the time, an 80% reduction of the overall node power consumption can be achieved in a typical sensor network setting. Comprehensive energy consumption comparisons between Medusa MK-2 nodes and other SN nodes designs can be found in [Sav02].

5.3 BWRC PICONODE

Another communication-centered sensor node design is the PicoNode [Rab00]. The main overall objective of this design is to simultaneously provide both flexibility and low energy consumption. It consists of four main modules. The first two units are processors: an embedded processor unit and configurable satellite units. The embedded processor is dedicated mainly for application and protocol-stack layers that require higher flexibility but have relatively low computational complexity and are infrequently requested. Configurable processing modules are targeted for the more frequent tasks with higher computational requirements. The other two modules are dedicated to communication tasks. They are a parameterized and configurable digital physical layer and a simple direct-down conversion RF front end.

These modules are interconnected by a flexible and low-power consumption interconnect scheme. The authors claim that a dynamic matching between application and architecture leads to significant energy savings for signal-

processing applications while maintaining implementation flexibility. One of the main premises of the design is the observation that the processor implementation is three orders of magnitude more expensive in terms of energy consumption than the implementations of the dedicated hardware. However, there is also the tradeoff between flexibility and programmability (software on programmable platforms) and energy consumption (ASIC hardware). The traditional approach is to design the wireless transceiver using only RF and analog circuit modules. More recently, a design approach that is mostly digitalized has emerged. This is inspired by the insight that digital circuits can improve exponentially with the scaling of technology, while analog circuits get linearly worse. This is mainly due to the reduction of the supply voltage. Therefore, it is beneficial to incorporate a small, noncritical analog front end and use digital back-end processing to balance the limitations.

Many design challenges are related to the physical layer. They are mostly related to the low-energy targets and variable demands from the network. Therefore, in order to satisfy various demands from the network, the PicoNode physical layer is parameterizable. These parameters include power control modes, modulation scheme, and bit rate. In order to meet the low-energy requirement, the physical layer must meet two mutually exclusive criteria: fast signal acquisition and low standby power. The first criterion is referring to the process of waking up in the least amount of time, then receive bursts of data and immediately go back to sleeping mode after the data acquisition. The second criterion emphasizes on consuming the least amount of energy while sleeping. The reason why they are usually mutually exclusive is that there exists an inverse proportional relationship between the depth of sleep (i.e. energy consumed) during standby and the time required to wake up.

PicoNode is designed in such a way that it does not require an interval power supply. It is self-constrained and self-powered using the environment by harvesting energy from light and vibrations [Rab00]. There are two major constraints for harvesting ambient energy from the environment: applicability within the environment and the size of the node (Berkeley group targets the one-cubic-centimeter design).

5.4 SENSOR-CENTRIC DESISGN: LIGHT COMPASS

The final sensor node design alternative that we will briefly overview is the light compass node [Won03]. The emphasis in this approach is completely shifted from computation, communication, and storage to sensors. The first

three functions are provided by a standard laptop or PDA. The rationale is that this type of design will progress on its own to become a viable platform for sensor network nodes. Even the interface of the sensor is built using off-the-shelf component. The focus is placed on sensors and how to select and place them in such a way that sensor data fusion is facilitated. In addition, special emphasis is place on how to rapidly develop retargetable sensor data fusion software and how to develop systematic procedures for design of sensor nodes.

Figure 1 shows the light sensor components used. The smallest device (on the left) is a miniature silicon solar cell that is used for converting light impulses directly to electrical charges (photovoltaic). It generates its own power and therefore does not require any external bias. This silicon cell is further mounted on a 0.78cm x 0.58cm x 0.18cm thick plastic carrier that generates roughly 400 mV in moderate light (most typical rooms). A significantly larger sensor (on the right), referred to as a photoconductor, measures 2.54cm x 2.15cm and can be surrounded by a 0.18cm thick plastic encapsulated ceramic package. In strong light its resistance measures 20O, and 5KO in complete darkness. These components are very economically viable (roughly $0.30 each) and they can be easily purchased in large quantities.

These sensors can be used in multiple prototypes such as the ones shown in figure2. On the left of Figure 2, the six-sided cut-pyramid structure has base length of 3 cm and a top edge length of 1 cm with a 60º slope. Sensor(s) can be attached to each side of the structure depends on the application and purpose. The structure on the right is a cube with 2cm edges, therefore it can incorporate up to six sensors with one on each surface.

In this light sensor platform, the heart component is an 8-channel analog to digital converter (ADC) module. It is used to read the sensor values through the parallel port of a standard PC laptop. This ADC component is comprised of a Maxim MAX186 ADC which has an internal analog multiplexer that can be configured for eight single-ended, or four differential inputs at a 12-bit resolution; with a conversion time that is under 10s. This component is pictured on the left in Figure 3. In addition, some of the other components of the circuit include: several resistors to protect the analog inputs; capacitors to filter noise; an external 4.096V voltage regulator; and an 8-bit digital latch required for parallel port communications. The overall design flow of a sensor appliance is presented in detail in Figure 4.

The main goal of this design was to achieve low power consumption while maintain a tolerable level of coverage. Figure 5 – 7 depict the results obtained from four different sensor structures: a 4-sensor pyramid (square base), a 4-sensor cut pyramid (triangular based pyramid with a flat sensor on top), a 5-sensors pyramid (pentagonal base), and a 5-sensor cut pyramid (square base pyramid with a flat sensor on top). In all cases, the objective was to estimate the positions of 5000 randomly placed light instances.

6. WIRELESS SNs AS EMBEDDED SYSTEMS

In this Section, we briefly survey the architecture of wireless SNs at the network level. For the networking of the wireless devices and appliances, several communication schemes have been proposed such as satellite, WLAN, cellular, and ad-hoc multihop architectures. Based on the different architectures, the communication between the nodes can be all low power (ranges in meter), high power (ranges in Mega meters) or medium power (ranges in Kilometers).

For example, wireless sensor networks are the widely used in cellular wireless networks. In this architecture, a number of base stations are already deployed within the field. Each base station forms a cell around itself that covers part of the area. Mobile wireless nodes and other appliances can communicate wirelessly, as long as they are at least within the area covered by one cell. An example of such a network is shown in Figure 8. The communication requires only medium power, although the fixed and immobile base stations are consuming a large amount of power to cover a large area and to communicate to and from the lower power mobile wireless nodes. However, the cellular wireless architecture has the drawback of not only having to be implanted in the field, but also it's cells should be carefully designed to have full coverage and transparency with respect to the cells.

Wireless local area networks (WLAN) are built for high frequency radio waves. The WLAN also need its own infrastructure within the designated local area. It is very well suited for local private areas such as offices, campuses and buildings. In some of the applications of the sensor network such as smart buildings, connecting the sensor networks to the WLAN implanted within the area is very suitable. The power consumption in LAN is also medium, although again, the fixed part of the infrastructure is naturally higher powered.

In order to overcome the difficulties caused by the infrastructure settings for wireless satellites, WLAN and cellular networks, a new generation of wireless networks architecture has emerged – the wireless multihop ad-hoc networks. In such networks, the infrastructure architecture is not needed and the nodes can configure themselves to communicate to other nodes within their communication range on the fly. The nodes are short range and therefore all of the communications are low power. If two nodes that are not within each other's range need to communicate to each other, they use the intermediate nodes as the relays. There are at least four reasons why the multihop ad-hoc wireless sensor network architecture appears as an attractive alternative to the WLAN and cellular technologies. The first reason is the on demand formation of the network does not require pre-deployed architecture. The second reason that multihop routing, can save orders of magnitude of power consumption when compared to the long range routing for the same distance [Rab00]. The third reason is the bandwidth. Since the communications between the nodes are short-range and local, the bandwidth is re-usable as opposed to the long-range communications. The fourth reason is the fault tolerance [Cer02]. Sensor network are envisioned to have a lot of inexpensive nodes embedded in the environment. The ad-hoc multihop architecture supports the advent of the new nodes and departure or failure of the old ones.

Most of the current sensor network literatures have been advocating the ad-hoc multihop architecture [Aky02] [Est99, Hil00, Kah00, Rab00, Ye02]. Nevertheless, there are no indications that the ad-hoc multihop architecture would be the best architecture for all of the sensor network applications. Because of the quantity of the radios and the number of the packets flowing in the network, there is a natural asymmetry in the multihop ad-hoc implementation. In fact, for some application such as smart buildings or scientific experimentations, where the network does not change over the space, having a number of static components in the network is natural solution. The static parts would be connected to the constant power supply, so that wireless parts can use low power to communicate to them and also nodes can go in the standby mode from time to time.

Another important issue related to the sensor networks is the topology of the network [Cer02]. The question is how to distribute the nodes within the field to achieve the best range and coverage from the sensors. This question is a variation of the well-known art-gallery problem [O'R87], where the new constraint on the nodes is that they have a short communication range. The other big issue in the topology consideration is that not all of the nodes should be

uniformly distributed, as is the assumption in the current literature and simulations for sensor networks. Furthermore, the network architecture should address the concerns of the various layers of the network. There is still a need for the better components in the physical layer [Kah99], power control and MAC layer [Ye02], and the routing protocols [Est99] at the network layer. The only proposed operating system for the sensor network is TinyOS that is an operating system at the node level [Hil00]. There is a need for a more complex network operating system (NOS) that can (1) facilitate the autonomous mode for the ad-hoc multihop architecture, (2) address the privacy and security concerns, and (3) provide efficient execution of the localized algorithms.

We conclude this Section with a very brief overview of three industrial wireless networks standards: IEEE 802.11b, Bluetooth, and HomeRF. IEEE 802.11b or WiFi primarily targets computer communication. Although it primarily targets indoor connectivity at speed of 11 Mbps within 150 m, it is expected that it will provide the same level of service outdoor within 300 m range. With specially equipped radios (amplifiers and special antenna) it may establish connectivity within 30+ km range. It can operate in several modes, including peer-to-peer and infrastructure access point. The wired equivalent privacy (WEP) standard ensures data protection using 40 and 128 bit RC4-based encryption.

Bluetooth mainly targets personal area networks on very short distances and applications such as audio, video, and multimedia. Both IEEE802.11b and Bluetooth use 2.4 GHz ISM band for unlicensed radio communication. HomeRF provides inexpensive residential-oriented wireless connectivity.

7. SUMMARY

We surveyed the architectural and synthesis issues related to sensor networks. The analysis has been conducted at three levels of abstraction: subsystem, individual node, and network. We identified the main design objectives, the current trends, and their relative advantages and limitations. Furthermore, several architecture and design case studies have been conducted. The special emphasis was placed on formulating the highest impact architectural and synthesis challenges.

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