

Holistic Optimization Framework for FPGA Accelerators

Stéphane Pouget

University of California, Los Angeles

pouget@cs.ucla.edu

Michael Lo

University of California, Los Angeles

milo168@ucla.edu

Louis-Noël Pouchet

Colorado State University

Louis-Noel.Pouchet@colostate.edu

Jason Cong

University of California, Los Angeles

cong@cs.ucla.edu

Abstract—Customized accelerators have transformed modern computing by delivering substantial gains in energy efficiency and performance through hardware specialization. Field-Programmable Gate Arrays play a critical role in this paradigm, offering unmatched flexibility and high-performance potential. High-Level Synthesis and source-to-source compilers have simplified Field-Programmable Gate Arrays design by translating high-level programming languages into hardware descriptions enriched with directives. However, achieving high Quality of Results remains a significant challenge, requiring intricate code transformations, strategic directive placement, and optimized data communication.

This paper presents *Prometheus*, a comprehensive framework that integrates key optimizations, including task fusion, tiling, loop permutation, computation-communication overlap, and concurrent task execution, into a unified design space. By leveraging Non-Linear Problem methodologies, *Prometheus* explores this design space to deliver efficient solutions under strict resource constraints, facilitating automatic bitstream generation. The framework addresses limitations in existing methods and demonstrates superior performance, achieving high Quality of Results across complex computation-bound applications.

I. INTRODUCTION

The rise of customized accelerators has transformed modern computing, delivering substantial improvements in energy efficiency and performance through hardware specialization. Field-Programmable Gate Arrays (FPGAs) have emerged as a particularly versatile solution, valued for their flexibility and ability to achieve high performance across diverse applications. High-level synthesis (HLS) tools and source-to-source compilers [9], [20], [31], [32], [37], [42], [49], [59], [61], [75], [76], [78]–[80] have simplified hardware design by translating high-level programming languages (e.g., C++, Python) enriched with hardware-specific directives into synthesizable hardware descriptions. However, the effectiveness of these tools depends heavily on the quality of the input code and the strategic application of hardware directives, making it challenging to achieve high Quality of Results (QoR) without significant manual effort.

Despite advancements in the field, designing optimized FPGA solutions remains a complex task. Existing approaches [9], [25], [31], [37], [57]–[59], [63], [65], [65], [66], [70], [77], [78], [81] often address specific aspects of FPGA design

in isolation, leaving gaps in areas such as efficient code transformation, effective concurrency management, and resource optimization. Moreover, challenges such as overlapping computation and communication, balancing intra-task parallelism, and managing FPGA resource constraints—including multi-Super Logic Region (SLR) architectures—further complicate the development process. These challenges are exacerbated by the lack of holistic frameworks that integrate multiple optimization strategies while ensuring synthesizable output.

Two commonly used paradigms—shared buffer and dataflow—have shown promise in improving FPGA performance. Shared buffers enable data reuse and promote parallelism by caching information on-chip, which is particularly beneficial for computation-bound kernels. However, their efficacy is often constrained by the limited on-chip memory, preventing full data caching and hindering the ability to overlap computation and communication effectively. On the other hand, the dataflow paradigm facilitates efficient data movement and task concurrency by leveraging FIFO (First-In-First-Out) communication. While this approach is effective for memory-bound kernels, it struggles to exploit shared memory and parallelism within tasks, and its independent task compilation can limit resource sharing opportunities.

This work addresses these challenges by focusing on optimizing HLS for FPGA design, with a particular emphasis on reducing latency while adhering to resource constraints. The goal is to transform affine high-level code (e.g., Listing 1) into an SLR-aware HLS-C++ design that achieves high QoR and facilitates automated bitstream generation. Achieving this requires addressing multiple challenges simultaneously, including task-to-SLR mapping, balancing computation and communication, and efficiently regenerating code to adapt to resource conflicts or spatial congestion. Existing methods fall short of providing an integrated solution capable of achieving these objectives, highlighting the need for a unified approach.

To address these limitations, we propose *Prometheus*, an integrated framework that combines the benefits of shared buffer and dataflow paradigms to optimize HLS-based FPGA design. The key contributions of this work include:

- A unified design space supporting tiled dataflow architectures, task fusion, tiling strategies, loop permutation, over-

lapping computation and communication, and concurrent task execution.

- The application of a Non-Linear Problem (NLP) formulation to discover optimal design parameters within strict resource constraints, enabling efficient bitstream generation.
- An end-to-end automated framework that generates OpenCL host code for correctness verification, performs Vitis HLS simulations, and produces the final bitstream.
- Rigorous evaluation through RTL simulation and on-board evaluation, demonstrating superior QoR compared to state-of-the-art tools like AutoDSE [66], Sisyphus [59], and ScaleHLS [78].

II. BACKGROUND AND MOTIVATION

A. HLS Optimization

HLS optimizations rely heavily on directives such as *unroll*, *pipeline*, and *array_partitioning*, which play a pivotal role in enhancing performance. The *unroll* pragma duplicates the loop body in the RTL design to enable parallel execution of loop iterations, while *pipeline* overlaps loop operations, reducing latency based on the initiation interval (II). Similarly, *array_partitioning* divides arrays into on-chip memory banks, allowing simultaneous access and facilitating more effective unrolling.

Advanced optimizations also leverage shared buffers to reduce off-chip memory transfers, ping-pong buffering to overlap data transfer and computation, and coarse-grained parallelism through duplicated processing elements [19]. Modern AMD/Xilinx FPGAs support data transfers with bit widths up to 512 bits, determined by problem dimensions. For instance, transferring 216 floats using a 256-bit width (8 floats per transfer) requires 27 transfers.

HLS tools like Vitis HLS support the *dataflow* pragma, which organizes computations into independent actors communicating through FIFO queues [40]. This structure enables concurrent execution by allowing each actor to process inputs and generate outputs as soon as data becomes available. Performance evaluations often combine estimation (e.g., Vitis HLS reports), RTL simulation, and on-board evaluation. While estimations and simulations avoid place-and-route overheads, on-board evaluations impose stricter constraints for generating deployable bitstreams.

B. Limitations of Existing Methods

The limitations of current HLS optimization frameworks are illustrated through the *3mm* kernel, which performs two independent matrix multiplications followed by a dependent multiplication. As shown in Listing 1, each matrix multiplication involves nested loops that can benefit from parallelism, unrolling, and communication-computation overlap.

Shared Buffer Frameworks such as AutoDSE [66], Sisyphus [59], ScaleHLS [78], and others [57], [58], [63], [65] optimize *3mm* primarily through sequential execution of matrix multiplications. This approach enables reuse of DSP resources but fails to leverage opportunities for concurrent execution, such as running the first two multiplications in parallel.

```

1 for (i = 0; i < 180; i++) // MM 1
2   for (j = 0; j < 190; j++) {
3     E[i][j] = 0.0; // S0
4     for (k = 0; k < 200; ++k)
5       E[i][j] += A[i][k] * B[k][j]; // S1
6 for (i = 0; i < 190; i++) // MM 2
7   for (j = 0; j < 210; j++) {
8     F[i][j] = 0.0; // S2
9     for (k = 0; k < 220; ++k)
10      F[i][j] += C[i][k] * D[k][j]; // S3
11 for (i = 0; i < 180; i++) // MM 3
12   for (j = 0; j < 210; j++) {
13     G[i][j] = 0.0; // S4
14     for (k = 0; k < 190; ++k)
15       G[i][j] += E[i][k] * F[k][j]; // S5

```

Listing 1. Code of *3mm*

Current frameworks transfer arrays at different loop levels to manage on-chip memory but lack automatic mechanisms to overlap computation with communication effectively.

Although shared buffering could support concurrent execution of independent tasks, its application remains limited. Extending concurrency to all three multiplications would require task fusion, which may constrain compiler optimizations.

Dataflow The dataflow paradigm, as implemented in frameworks like StreamHLS [9], divides computations into independent tasks, with communication managed through FIFOs. For the *3mm* kernel in Listing 1, dataflow enables concurrent execution of the first two matrix multiplications, while the third begins as soon as its inputs are ready. This approach overlaps computation and communication, effectively managing task dependencies. As *3mm* is computation-bound, increasing parallelism is essential. However, parallelism in pure dataflow methods is constrained by the FIFO bit width of the receiving task and the number of FIFOs. Increasing FIFO bit widths or adding more FIFOs to handle higher concurrency often results in routing congestion, making it challenging to generate a valid bitstream. Additionally, the lack of shared memory prevents data reuse across tasks, leading to repeated off-chip transfers or redundant buffers.

Mixed Methods Mixed approaches, such as those used by Allo [15] and HIDA [77], combine shared buffering and dataflow paradigms. Allo extends HeteroCL [37] within the MLIR framework [39], supporting code transformation and dataflow scheduling. However, these methods lack automatic data-tile selection and pragma insertion, limiting their ability to optimize QoR effectively.

General Limitations Most existing HLS frameworks fail to address key challenges such as automatic ping-pong buffering, tile size adjustments, and padding to maximize bit widths for communication efficiency. Unroll factors are often restricted to evenly divide problem dimensions, which can lead to inefficiencies with partial tiles. Expanding these factors and incorporating dynamic adjustments could significantly enhance parallelism and performance.

C. Overview of Prometheus

We present Prometheus, a unified optimization framework designed to efficiently explore design spaces using a Non-

Linear Problem (NLP) cost model. Prometheus simplifies the development of FPGA designs by offering an engineer-friendly interface with adjustable parameters such as tile size, array partitioning, and unroll factors. It is SLR-aware, ensuring effective task distribution across Super Logic Regions (SLRs), which simplifies bitstream generation while optimizing the balance between performance and resource utilization.

The pseudo-code in Listing 2 demonstrates how Prometheus processes the *3mm* kernel. Load and store operations manage data transfers to and from off-chip memory, while send and receive operations handle inter-task communication using FIFO.

Each *task_i* in the pseudo-code corresponds to the fully unrolled computation of an intra-tile for statement *S_i* in Listing 1. An example of such a task is illustrated in Listing 3.

Arrays *E*, *F*, and *G* are initialized to zero within their respective tasks (e.g., S0, S2, and S4) and are not preloaded, reducing unnecessary memory overhead.

Prometheus enhances computation efficiency by fusing statements that produce the same outputs (e.g., in Listing 1), and it automatically formulates an NLP problem to determine the theoretically optimal parameters, such as loop schedules, array bit widths (e.g., 512 bits), tile sizes, reuse buffer sizes, transfer locations, and padding. The framework dynamically adjusts bit widths for arrays like *F*, *D*, and *G* to achieve a better balance between parallelism and resource usage.

```

1 /***** Fused Task 0 *****/
2 float B[204][192]; load_B(B);
3 for (i0 = 0; i0 < 18; i0++){//inter-tile loop
4     float A[10][204]; load_A(A);
5     for (j0 = 0; j0 < 6; j0++){//inter-tile loop
6         float E[10][32];
7         task0(E); // S0 + intra-tile loops
8         for (k0 = 0; k0 < 51; ++k0)//inter-tile loop
9 #pragma HLS pipeline II=3
10            task1(E, A, B); // S1 + intra-tile loops
11            store_E(E); sent_E(E);
12 /***** Fused Task 1 *****/
13 float C[190][222]; load_C(C);
14 for (j0 = 0; j0 < 7; j0++){//inter-tile loop
15     float D[222][32]; load_D(D);
16     for (i0 = 0; i0 < 10; i0++){//inter-tile loop
17         float F[19][32];
18         task2(F); // S2 + intra-tile loops
19         for (k0 = 0; k0 < 74; ++k0)//inter-tile loop
20 #pragma HLS pipeline II=3
21            task3(F, C, D); // S3 + intra-tile loops
22            store_F(F); sent_F(F);
23 /***** Fused Task 2 *****/
24 float E[180][192];
25 for (j0 = 0; j0 < 7; j0++){//inter-tile loop
26     float F[192][32];
27     receive_F(F);
28     for (i0 = 0; i0 < 18; i0++){//inter-tile loop
29         float G[10][32];
30         receive_E(E);
31         task4(G); // S4 + intra-tile loops
32         for (k0 = 0; k0 < 32; ++k0)//inter-tile loop
33 #pragma HLS pipeline II=3
34            task5(G, E, F); // S5 + intra-tile loops
35            store_G(G);

```

Listing 2. Pseudo Code of *3mm* generated by Prometheus

Efficient computation-communication overlap is achieved through ping-pong buffering, while concurrent task execution and FIFO-triggered dependent tasks maximize overall performance. Fused Tasks 0 and 1 execute concurrently, while Fused

Task 2 begins as soon as the data tiles for *F* and *E* become available.

For the *3mm* kernel optimized with RTL simulation, Prometheus achieved a throughput of 368.36 GF/s, significantly surpassing state-of-the-art frameworks such as Sisyphus (178.97 GF/s), Allo (60.40 GF/s), ScaleHLS (43.04 GF/s), and AutoDSE (1.74 GF/s). These results demonstrate the effectiveness of Prometheus in overcoming the limitations of existing methods and achieving superior QoR.

III. CODE TRANSFORMATION

In our dataflow model, we adopt a synchronous dataflow where the sizes of the arrays are known during compile time. This compile-time awareness enables us to construct a precise model that facilitates rigorous optimizations. To leverage FPGA parallelism, we implement an acyclic dataflow graph, ensuring parent nodes do not receive data from their children. While this constraint limits graph configurations and may increase resource usage, it reduces overall latency. To support this structure, we inline [16] each function in the input code to generate the required acyclic graph. Our primary objective is to minimize latency within resource constraints by overlapping communication and computation within tasks and executing independent tasks concurrently. To achieve this, we apply various transformations and optimizations, explored in this section, and navigate the design space using an NLP-based approach, detailed in Section IV.

Dependency Graph Creation Our process starts with affine C/C++ code as input, which undergoes maximal distribution to ensure each loop body contains only one statement, provided no dependencies exist within the loop. ISCC [68] verifies the legality of these transformations, ensuring dependencies are preserved. After achieving full distribution, we construct a dependency graph using PoCC [53]. PoCC provides the necessary information about the schedule and dependencies, enabling us to build the graph. In this graph, the nodes represent tasks, while the edges capture data communication arising from inter-task dependencies. Tasks with identical outputs are then merged (when legal), creating fused tasks with output-stationary properties. This ensures that each tile’s output is handled (loaded, computed, and either stored or transmitted) only once. If a dependency prevents distribution, the framework will still function but with a more limited optimization space, making it more effective when distribution is possible.

Prometheus’s solution space includes:

Data-tiling and Padding In the fused dependency graph, edges represent data communication between tasks as well as between tasks and off-chip memory, involving the transfer of data tiles with specified sizes. Data tiling divides loop iterations into smaller tiles, splitting array accesses into subsets. Each loop *l* iterating over an array *a* is divided into an outer loop (TC_{inter}^l) and an inner loop (TC_{intra}^l), with feasible permutations applied. For each array and dimension iterated by the loop *l*, the tile factor is a common choice that influences all arrays iterated by this loop.

To optimize memory transfers, padding is applied to arrays in two ways. Simple padding increases the bit width (BW_a) for efficient transfers while maintaining the original loop trip count. Composite padding adjusts both BW_a and the loop trip count (TC^l) to support unroll factors that do not evenly divide the original trip count, allowing irregular tile sizes and expanding the design space. Tile sizes are consistent within a fused task but vary between tasks. In Listing 2, the tile size of array F is 19×32 in Fused Task 1 and 192×32 in Fused Task 2.

Fine-grained Parallelism Data-tile selection involves splitting each loop and permuting them to create two levels of the original loops. Using ISCC [68], we verify the legality of these permutations, resulting in two loop levels: inter-tile (outer) and intra-tile (inner). If permutation is not feasible, the inter-tile loop retains its legal position. For tasks belonging to the same fused task, we merge their inter-tile loops, which are non-reduction. For instance, in Listing 2, the inter-tile loops on lines 3 and 5 iterate over task0 and task1. The intra-tile loops are fully unrolled, ensuring that all data accesses within the intra-tile remain on-chip. Array partitioning, determined by the unroll factor, ensures data resides in separate BRAM banks for simultaneous access. Reduction loops across inter-tiles are pipelined with an initiation interval ($II = n > 1$), where n matches the reduction latency. For instance, in Listing 2, additions take 3 cycles, resulting in $II = 3$.

Loop Order Due to the full unrolling of the intra-task, there is no need to select the loop order within the intra-tile. We place the inter-tile reduction loops directly above the task and are pipelined. If multiple reduction loops exist, we rank them by the size of their trip counts, placing the loop with the highest trip count innermost to ensure an efficient pipeline. This setup provides the flexibility to choose the order of the inter-tile loops that are not reduction loops. This order will subsequently be determined by the NLP (cf. Section IV). As shown in Listing 2, the loop order of Fused Tasks 1 and 2 is permuted compared to the original program in Listing 1.

Automatic Overlapping of Communication and Computation To overlap communication and computation, we use on-chip buffers. The buffer size and data transfer location are determined by various options explored via NLP (cf. Section IV). Since data must stay on-chip for intra-task computation, transfers occur either below an inter-tile loop or before any loops start. The transfer position determines the data tile size, covering all data accessed below it. To improve data reuse, buffer size can match or exceed the transferred data tile. Similar to transfer location, buffer size is determined by its position relative to inter-tile loops or before any loops. Two boolean variables, $d_{a,l}$ and $t_{a,l}$, define and transfer array a under loop l when set to true. If defined or transferred before loops, $l = 0$. Double-buffering is used for read-only or write-only arrays, and triple-buffering for arrays that are both read and written. Following [19], we perform an initial load, then overlap loading the next tile with computing the current one.

Coarse-Grained Parallelism: Automatic Execution of Concurrent Tasks Due to the use of the dataflow pragma,

tasks can begin computation as soon as they have sufficient data, allowing for concurrent execution. This concurrency significantly increases overall performance.

Memory Transfer Communication latency is reduced by transferring more data per cycle using increased bit width with padding. Read-only arrays are duplicated in off-chip memory for tasks with multiple reads, eliminating feed-through logic. For non-read-only arrays, data passes between tasks via FIFOs, using the same bit width as for off-chip memory transfer.

IV. NLP FORMULATION

To determine the tile size, loop order, bit width, and memory transfers, we formulate a cost model as a NLP problem aimed at minimizing overall latency. This approach builds upon the methodology proposed by Pouget et al. [57]–[59], which we have adapted to address our specific requirements and constraints. In our work, we incorporate dataflow considerations along with all the optimizations detailed in Section III. We employ PoCC [53] to extract compile-time information such as schedules, loop trip counts, dependencies, and operation counts per statement. ISCC [68] then generates all legal permutations for each loop body.

Table I delineates the sets, variables, and constants utilized in our NLP formulation.

Constants	Description
II_l	II of the loop l
IL_{par}	Iteration Latency of the operations without (<i>par</i>) and with (<i>red</i>) dependencies of the statement s
IL_{red}	
TC_{ori}^l	Original Trip Count of the loop l
$f_{a,l}$	Footprint of the array a if transferred to on-chip after the loop l
N_{FT}	Number of fused task
DSP_{sop}	Number of DSP used by the statement s for the operation op
DSP	Number of DSP available for the FPGA used
max_{part}	Maximum array partitioning
SLR	Number of SLR available for the FPGA used
Variables	Description
TC_{intra}^l	TC of the loop l for the intra and inter tile
TC_{inter}^l	
TC^l	Trip Count of the loop l after padding
S_a^{last}	Size of the last dimension of the array a transferred on-chip
BW_a	Bit width of the array a
$t_{a,l}, d_{a,l}$	Boolean to know if the array a is transferred and defined (respectively) on-chip after the loop l in the inter-tile
p_i^l	Position of the loop l under the i -th permutation
slr_t	ID of the SLR use by the task t
Sets	Description
$\mathcal{L}, \mathcal{A}, \mathcal{S}$	The set of loops, arrays and statements
\mathcal{L}_s	The set of loops which iterate the statement s
\mathcal{L}_{red}^s	The set of reduction loops which iterate the statement s
\mathcal{L}_a^{last}	The set of loop which iterate the last dimension of the array a
\mathcal{L}_{inter}	The set of loops which belong to the inter-tile and intra-tile respectively
\mathcal{L}_{intra}	
\mathcal{B}	Set of possible burst size for the data type
$\mathcal{C}_{a,d}$	The set of loops which iterates the array a at the dimension d
$AP_{a,d}$	Array Partition for the array a in dimension d
\mathcal{P}_s	All permutation of the loops which iterate the statement s
\mathcal{F}_i	The set of statements which belong to the fused task i
\mathcal{T}	The set of tasks in the dataflow

TABLE I
OVERVIEW OF THE CONSTANT, VARIABLE AND SET EMPLOYED IN FORMULATING THE NLP

```

1 for (int j1 = 0; j1 < 32; j1++) {
2 #pragma HLS unroll
3   for (int i1 = 0; i1 < 19; i1++) {
4 #pragma HLS unroll
5     for (int k1 = 0; k1 < 3; k1++) {
6 #pragma HLS unroll
7       j=j0*32+j1; i=i0*19+i1; k=k0*3+k1;
8       F[i1][j1] += C[i1][k] * D[k][j1];}

```

Listing 3. Pseudo Code of the task₃

A. Constraints

We now describe the constraints by using the code of Listings 1, 2 and 3.

Data-tiling and Unroll Factor The intra-tile transformation, as explained in Section III, can divide either the original loop trip count or the original trip count with padding, thereby increasing the range of possibilities. Equation 1 ensures that the trip count of the intra-tile is a divisor of one of these two possibilities. The user has the option to constrain the padding using Equation 2, which simplifies the solution space for the NLP solver. For instance, in Listing 3, for the array F , the loop j (line 7 in Listing 1) has been split into $j0$ (line 14 in Listing 2) and $j1$ (intra-tile). The trip count of the intra-tile loop $j1$, denoted as $TC_{intra}^{j1} = 32$, does not evenly divide the original trip count $TC_{ori}^j = 210$, but it does divide the trip count of the padded loop $TC^j = 224$.

$$\forall l \in \mathcal{L}, TC_{intra}^l \% TC_{ori}^l == 0 \mid TC_{intra}^l \% TC^l == 0 \quad (1)$$

$$(opt) \forall l \in \mathcal{L}, \exists n \in \mathbb{N} \leq N \in \mathbb{N}, \text{ s.t. } TC^l = TC_{ori}^l + n \quad (2)$$

Bit Width B denotes the number of elements that can be transferred simultaneously, determined by the bit width and the data type. Hence, if we have a bit width under 512 bits for *float* the set is $\{1, 2, 4, 8, 16\}$. Equation 3 computes the bit width for each array based on the last dimension of the data-tile transferred on-chip. For example, the array D in Fused task 1 is transferred in line 15 with a size of 222×32 , so $S_D^{last} = 32$, which is divisible by 16. Therefore, it has a bit width of 16.

$$\forall a \in \mathcal{A}, \forall l \in \mathcal{L}_a^{last}, \max_{b \in \mathcal{B}} BW_a = b \text{ s.t. } S_a^{last} \% b = 0 \quad (3)$$

Permutation Equation 4 requires the NLP to choose identical permutations for loops that are shared by statements fused within the same task. For example, in Fused task 1, the loops iterating statement S2 can be permuted as $(i0, j0)$ or $(j0, i0)$, and similarly, loops iterating statement S3 can be permuted as $(i0, j0)$ or $(j0, i0)$. However, since the loops $i0$ and $j0$ iterate both S2 and S3, they must use the same permutation; either $(i0, j0)$ for both or $(j0, i0)$ for both.

$$\begin{aligned} & \forall i \in \llbracket 0, N_{FT} \rrbracket, \forall (ft_0, ft_1) \in \mathcal{F}_i^2, \\ & \forall (i_0, i_1) \in \mathcal{P}_{ft_0} \times \mathcal{P}_{ft_1}, \forall l \in \mathcal{L}, p_{i_0}^l = p_{i_1}^l \end{aligned} \quad (4)$$

Transfer and Reuse Equation 5 permits the selection of a single level where each array can be defined (and reused) and transferred. Equation 6 constrains that the definition of the array must occur lexicographically before or at the same time as the transfer.

The array E , defined on line 24 in Listing 2, is defined before any loops, so $d_{E,i0} = 1$ (0 indicating it is defined before

any loops). However, it is transferred under the loop $i0$, so $t_{E,i0} = 1$. Equation 6 simply means that the definition of array E should occur before or at the same level as the transfer. We cannot transfer E under loop $i0$ if E is defined under $k0$. Similarly, in Listing 2, the array A is defined and transferred in line 4, with $d_{A,i0} = 1$ and $t_{A,i0} = 1$.

$$\forall a \in \mathcal{A}, \sum_{l \in \mathcal{L}_{inter}} t_{a,l} = 1, \sum_{l \in \mathcal{L}_{inter}} d_{a,l} = 1 \quad (5)$$

$$\forall a \in \mathcal{A}, \sum_{(l_0, l_1) \in \mathcal{L}_{inter}^2} d_{a,l_0}, t_{a,l_1} = 1, \text{ then } l_0 \preceq l_1 \quad (6)$$

On-chip Memory Equation 7 constrains the footprint of the array to be within the available resources, based on where the array is defined, the number of double buffers used and the footprint of the array transferred at this level.

$$\sum_{a \in \mathcal{A}} \sum_{l \in \mathcal{L}} d_{a,l} \times f_{a,l} \times N_a \leq Mem, \quad (7)$$

with N_a being the number of double buffer for the array a .

Array Partitioning Equation 8 limits the maximum partitioning of each array. This partitioning is crucial as it impacts the maximum unroll factor, necessitating the distribution of data across different BRAM banks under fully unrolled loops, thereby influencing the utilization of BRAMs. Equation 9 computes the array partitioning needed for each array based on the trip count of the fully unrolled intra-tile loops.

Array D in Listing 3 is traversed by two unrolled loops: $k1$, which iterates 3 times ($AP_{D,0} = 3$), and $j1$, which iterates 32 times ($AP_{D,1} = 32$). Therefore, the total number of partitions needed is $3 \times 32 = 96$. Consequently, these 96 values of F are stored in different banks, allowing all of them to be accessed in parallel. However, this value must be less than or equal to max_{part} .

$$\forall a \in \mathcal{A}, \prod_{d \in \mathbb{N}} AP_{a,d} \leq max_{part} \quad (8)$$

$$\forall a \in \mathcal{A}, \forall d \in \mathbb{N}, \forall l \in C_{a,d}, AP_{a,d} = TC_{intra}^l == 0 \quad (9)$$

DSP Utilization Equation 10 constrains the number of DSPs used based on the available DSP resources. In contrast to [57]–[59], we utilize pessimistic DSP utilization. This approach is necessary because concurrent execution and resource reuse between tasks are not feasible when two tasks can run simultaneously. Given $DSP_+ = 2$, $DSP_* = 3$, and $II_{S3} = 3$, the DSP usage for Task 3 is calculated as $(2 + 3) \times 1824$, accounting for the unroll factor. However, since the loop is pipelined with $II = 3$, the HLS compiler optimizes resource usage, effectively reducing the DSP count by approximately dividing by II .

$$\sum_{op \in \{+, -, *, /\}} \sum_{s \in \mathcal{S}} (DSP_{s_{op}} / II_s) \times \prod_{l \in \mathcal{L}_j} TC_{intra}^l \leq DSP \quad (10)$$

SLR Selection For each task, the NLP determines the SLR on which the task will be implemented (Equation 11). Additionally, Equations 7 and 10 are applied to each SLR to manage resource allocation per SLR effectively.

$$\forall t \in \mathcal{T}, slr_t \in \llbracket 0, SLR \rrbracket \quad (11)$$

B. Objective Function

The objective function models the dependency graph of the fused task. Independent tasks execute simultaneously, with latency set by the longest task. Dependent tasks overlap partially, with the second task starting once it receives enough data from the first. The latency is the maximum of both tasks' durations plus the "shift", the interval before the second task starts. For our 3mm example, the graph is shown in Figure 1, and the corresponding latency is:

$$\left\{ \begin{array}{l} Lat(T_0, T_1) = \max(Lat(T_0), Lat(T_1) + shift_{T_0, T_1}) \\ Lat(T_2, T_3) = \max(Lat(T_2), Lat(T_3) + shift_{T_2, T_3}) \\ Lat(T_0, \dots, T_4) = \max(Lat(T_0, T_1), Lat(T_2, T_3), Lat(T_4)) \\ Lat = \max(Lat(T_0, \dots, T_4), Lat(T_5) \\ \quad + \max(shift_{T_1, T_5}, shift_{T_3, T_5}, shift_{T_4, T_5})) \end{array} \right.$$

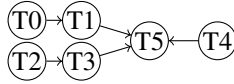


Fig. 1. Dataflow graph of 3mm maximally distributed

The latency of the intra-task for a statement s is determined similarly to [57]–[59] with Equation 12. And if the intra-task is iterated by the reduction loops in the inter-tile the latency is represented by Equation 13.

$$Lat_{intra} = IL_{par} + IL_{seq} \times \log_2 \left(\prod_{l \in \mathcal{L}_s^{red}} TC_{intra}^l \right) \quad (12)$$

$$Lat = Lat_{intra} + II \times \left(\prod_{l \in \mathcal{L}_s^{red}} TC_{inter}^l - 1 \right) \quad (13)$$

For each level $n \geq 0$ (with the outermost level being 0) of the inter-tile, we consider the shifting of load, compute, and store operations to enable overlapping of computation and communication. The overlap factor α is set to 1 for read-only operations and 2 for read and store operations:

$$Lat_n = \max(Lat_{n+1}, \frac{f_{a,l}}{BS_a}) + Lat_{n+1} + \frac{f_{a,l}}{BS_a} \times \alpha \quad (14)$$

And then, the final objective function is computed using the dataflow graph, where the latency of the task is established by the latency of the outermost level, denoted as Lat_0 .

V. CODE GENERATION

Prometheus takes as input affine C/C++ code and automatically produces an HLS-C++ file, OpenCL host files, and all necessary files for code verification, RTL simulation, and bitstream generation. The NLP described in Section IV gives the parameters of the space such as loop order, tiling factor, etc. However, in order to be efficient, the code generation needs some specific rules.

Communication with Off-Chip Memory To enable overlapping communication and computation, a *load* function transfers data on-chip using FIFOs, ensuring effective overlap management by the compiler. Furthermore, to guarantee that the *load* operation transfers data with the correct bit width, we automatically restructure the data in off-chip memory to

enable sequential loading. Once data accumulates in the FIFO, a *read* function moves it to the shared data-tile buffer, whose size is determined by the NLP. For outputs, a *write* function transfers data from the buffer to a FIFO, and a *store* function writes it back to off-chip memory.

Communication between the Fused Task The communication within the same fused task is not required as they use shared buffers. Similarly, for communication with off-chip memory, we choose to use FIFOs to facilitate communication between fused tasks, thereby simplifying the overlap.

Intra-Task Each intra-task, corresponding to an intra-tile selected by the NLP, is implemented as a fully unrolled, independent function without communication with off-chip memory. Data for these tasks resides entirely on-chip.

If the task involves reduction loops, inter-tile reduction loops are integrated into the function and pipelined. While the pipeline initiation interval (II) is greater than 1 due to reduction dependencies, other operations in the statement are pipelined efficiently.

Padding is handled at the intra-tile level. Non-reduction loops remain unchanged, allowing computation of padding values without excessive resource usage. For reduction loops, full tiles are computed first, and the intra-tile loop is adjusted to handle padding for partial tiles accurately.

Inter-Tile Loop For each fused task and each inter-tile loop, we generate independent functions to facilitate efficient double or triple buffering. Using information from the NLP, we determine which arrays are defined and which are transferred at each level of granularity. Once we identify the data being transferred, we implement double buffering if only reads or writes are involved, or triple buffering if both reads and writes are required. This strategy allows us to overlap the operations of reading, storing, and computing at the innermost level, optimizing both communication and computation overlap.

Concurrent Execution Using the *dataflow* pragma, independent tasks execute concurrently without requiring manual rewrites. Computation in a receiving task begins as soon as its shared buffer contains sufficient data.

SLR Management The NLP determines the SLR ID for each task, specifying where it will be executed. Prometheus generates a separate C++ file for each SLR, and data transfers between SLRs are managed via *ap_axiu* streams, ensuring efficient communication and minimizing transfer overhead.

VI. EVALUATION

A. Setup and Experimental Evaluation

We evaluated our method using kernels from Polybench/C 4.2.1 [55] with medium-sized datasets and single-precision floating-point computations. The selected kernels represent both memory-intensive and computation-intensive scenarios. Medium problem sizes were chosen to balance demonstration of efficacy and the feasibility of time-consuming RTL evaluations. NLP problems were solved using the AMPL description language and the Gurobi solver (version 11.0.0) with the *qp:nonconvex=2* option for non-convex quadratic objectives

and constraints. Evaluations included RTL simulation and on-board execution using the Alveo U55C FPGA, with a targeted frequency of 220 MHz. RTL simulation provided accurate latency estimates, contrasting with the overly optimistic Vitis HLS reports that assume perfect task overlapping with dataflow pragma. The generated code from the frameworks are compiled using AMD/Xilinx Vitis HLS 2023.2 using the Vitis flow [4]. This flow assumes that data initially resides off-chip and has a default latency of 64 cycles to bring onto on-chip memory. All frameworks utilize "unsafe math" optimizations, enabling commutative/associative reduction operations at the expense of precision.

The objective of this evaluation is to demonstrate the capability of our framework to generate code with high QoR, whether for memory-bound or computation-bound kernels. To achieve this, we compare our work with Allo, ScaleHLS, Sisyphus, and AutoDSE. We do not include a comparison with Stream-HLS [9] due to the unavailability of its source code. For ScaleHLS [78] and Allo [15], we apply the same method as our framework by padding memory transfers to attain the maximal bit width (512 bits) from off-chip to on-chip memory. Their kernels assume data are already in on-chip memory, so we modified their code to include off-chip to on-chip data transfers. Allo's *2mm* and *3mm* kernels already handle this transfer, requiring no modifications. We left Sisyphus and AutoDSE unchanged, as they already optimize bit width according to the problem size. We use AutoDSE with the bottleneck method, setting a DSE timeout of 1,000 minutes and an HLS synthesis timeout of 180 minutes per task. For Allo-generated designs, we utilize kernels from their artifact repository since Allo does not employ a DSE [1]. Sisyphus generated designs are generated using parameters consistent with the paper [59], and ScaleHLS designs are compiled using their open-source compiler [2]. For RTL simulation, we assume that the frameworks can utilize all the resources on the U55C FPGA with a constraint of partitioning any array of 1,024 due to AMD/Xilinx limitations. For on-board FPGA evaluations, we consider two scenarios. The first scenario utilizes 60% of one Super Logic Region (SLR), equivalent to 20% of total board resources, for all frameworks. The second scenario is unique to our framework, leveraging all three SLRs, with 60% utilization per SLR. Most frameworks are not place-and-route aware, leading to congestion issues that prevent bitstream generation. Limiting frameworks to one SLR increases the likelihood of meeting timing requirements. AutoDSE, for instance, lacks dataflow support and applies pragmas within a single function, making multi-SLR bitstream generation impossible without manual intervention to split the function across SLRs. If congestion persists within an SLR, we adjust the NLP constraints to address the issue and regenerate the HLS-C++ file in just a few minutes.

B. Comparison

The average time to solve the NLP and generate the designs presented in this section is 31.70 seconds, with a maximum of 178.41 seconds for *3mm* with 3 SLRs.

RTL Simulation Table II presents the RTL simulation results for Prometheus, Sisyphus [59], AutoDSE [66], ScaleHLS [78] (S-HLS), and Allo [15]. The last lines show the average and geometric mean performance improvement (PI) of Prometheus across evaluated kernels. Results marked with * are from the Vitis HLS report, showing minimum latency as an optimistic estimate. The RTL simulation for *3mm* with Allo was incomplete after two days.

Prometheus consistently achieves superior QoR across all evaluated kernels compared to other frameworks. While Sisyphus [59], designed primarily for computation-bound kernels, demonstrates competitive results for these kernels, it shows a weakness for *2mm* and *3mm*. This disparity is due to Sisyphus lacking concurrent execution capabilities for independent matrix multiplications. The performance advantage of Prometheus stems from both concurrent task execution and efficient overlapping of computation and communication.

Kernel	Ours	Sisyphus	S-HLS	Allo	AutoDSE
2mm	308.38	195.09	37.13	46.58	0.41*
3mm	368.36	178.97	43.04	60.40*	1.74*
Atax	3.56	2.32	1.58	1.96	1.97*
Bicg	15.41	2.32	1.70	14.17	0.99*
Gemm	419.14	227.09	40.53	37.50	110.81*
Gesummv	10.21	2.28	1.78	8.85	1.98*
Mvt	14.65	5.54	7.39	8.77	7.80*
Symm	212.20	200.30	0.06	16.72	14.68*
Syr2k	133.77	75.01	0.04	20.59	12.35*
Syrk	316.25	211.00	0.54	41.11	23.16*
Trmm	193.47	166.72	0.07	5.10	0.02*
PI (Avg)		2.39x	927.20x	8.58x	973.14
PI (gmean)		2.03x	48.03x	4.92x	25.82

TABLE II
COMPARISON OF THE THROUGHPUT (GF/S) WITH RTL SIMULATION

Although for *bicg*, Allo and Prometheus do not use the same code transformation, the results are similar. Allo retains the original code structure by permuting the reduction loop outermost. The non-reduction loop is fully unrolled, and the reduction loop is pipelined. Prometheus partially unrolls both loops and pipelines the reduction loop.

On Board Evaluation Table III presents the results for the on-board evaluation. The column $T(ms)$ indicates the kernel execution time in milliseconds, GF/s represents the throughput in Giga Floating Operations per second, and the resource usage is detailed in the thousands for both LUTs (L) and FFs. URAM utilization is excluded as no kernels use it. Column F (MHz) shows the frequency achieved by each design, with a target frequency of 220 MHz for all designs.

For *Bicg* and *Atax*, targeting 60% of resources on one SLR caused congestion, requiring regeneration with a 55% constraint. The *3mm* bitstream from AutoDSE succeeded only with a 15% constraint.

Prometheus achieves a remarkable 77.16x performance improvement over AutoDSE. This gain is accompanied by an average increase in resource utilization: 2.38x more DSPs, 1.08x more BRAM, 1.36x more LUTs, and 1.42x more FFs, reflecting the trade-offs made to achieve such high efficiency. When compared to Sisyphus, Prometheus demonstrates a

	Kernel	T (ms)	GF/s	DSP	BRAM	L(K)	FF(K)	F (MHz)
1 SLR Sisypus	2mm	1.20	30.57	556	510	213	276	220
	3mm	1.52	29.89	984	611	230	300	220
	Atax	0.62	1.03	173	450	240	250	220
	Bicg	0.63	1.02	173	451	238	265	217
1 SLR AutoDSE	2mm	92.25	0.40	963	353.5	287	292	205
	3mm	110.34	0.41	1117	470	278	306	220
	Atax	2.88	0.22	452	630.5	170	212	220
	Bicg	1.13	0.56	196	867.5	168	217	214
1 SLR Ours	2mm	0.56	65.13	1941	635.5	371	454	216
	3mm	0.87	51.95	1551	635.5	342	423	220
	Atax	0.24	2.62	1081	533.5	234	287	184
	Bicg	0.15	4.04	732	311.5	250	302	220
3 SLR Ours	2mm	0.29	125.54	2752	546	428	549	220
	3mm	0.34	134.07	4379	600	684	840	207
	Atax	0.20	3.10	1823	634.5	405	539	137
	Bicg	0.14	4.34	1226	241	291	380	177

TABLE III
ON-BOARD EVALUATION COMPARISON

notable 2.59x performance boost, leveraging an average of 3.88x more DSPs, 1.04x more BRAM, 1.31x more LUTs, and 1.33x more FFs, illustrating its ability to deliver substantial improvements while effectively utilizing additional resources.

Table IV shows the parameters found by the NLP. We use the same name of the iterator as Polybench 4.2.1 [55] code. S_i represent the statement in position i in the code. The second column gives the statement fused inside the same tasks, the third column sets the fused task order and loop order found by the NLP for the fused task and the last column supplies the data-tile size found by the NLP, if the array is present in a different fused task the fused-task (defined in the second column) is precise.

Permutations are evident in the implementations of *3mm*, *Atax*, and *Bicg*. For *2mm* and *3mm*, the NLP opted to fully transfer array B instead of overlapping computation and load, as the load operation had higher latency than computation. In *2mm*, the NLP retains the original loop order. Array *tmp* is transferred from the first task to the second, with both tasks iterating over the first dimension using loop i . This enables a 4×32 data tile to be sent to the second task, which starts computation once a 4×192 tile of *tmp*(FT1) is filled.

	Fused ment	State- ment	Loop Order	Data Tile Size
2mm	FT0: S0, S1, FT1: S2, S3		FT0: i,j,k, FT1: i,j,k	<i>tmp</i> (FT0): 4×32 , B: 212×192 , A: 4×212 , D: 4×32 , C: 192×32 , <i>tmp</i> (FT1): 4×192
3mm	FT0: S0, S1, FT1: S2, S3, FT2: S4, S5		FT0: i,j,k, FT1: j,i,k FT2: j,i,k	E(FT0): 9×16 , A: 9×200 , B: 200×192 , F(FT1): 10×10 , C: 10×224 , D: 224×10 , G: 9×10 , E(FT2): 9×192 , F(FT2): 192×10 , <i>tmp</i> (FT0): 56 , y: 16 , A(FT0): 392×416 , A(FT1): 392×16 , <i>tmp</i> (FT1): 392×16 , A (FT0): 416×16 , r: 416 , q: 10 , A (FT1): 10×400 , p: 400 ,
Atax	FT0: S1, S2, FT1: S0, S3		FT0: i,j, FT1: j,i	
Bicg	FT0: S1, S2, FT1: S0, S3		FT0: j,i FT1: i,j	

TABLE IV
FUSION, LOOP ORDER AND DATA-TILE SIZE FOUND BY THE NLP FOR THE KERNEL EVALUATED ON TABLE III FOR 1 SLR

As other frameworks cannot generate bitstreams for 3

SLRs without human intervention, we compare results for 1 and 3 SLRs using our framework. For *2mm* and *3mm*, performance improves due to increased resource utilization. However, for *atax* and *bicg*, where the bottleneck is memory transfer between off-chip and on-chip rather than parallelism, the improvement is negligible.

VII. RELATED WORK

Dataflow Dataflow principles have been extensively studied in models such as Kahn Process Networks [34], Dennis Dataflow [23], synchronous dataflow languages [12], [41], and for FPGA applications [3], [5], [11], [13], [15], [26], [52], [74]. DaCe [11] introduces Stateful DataFlow multiGraphs to separate program definition from optimization, enabling transformations like tiling and double-buffering, though requiring user intervention. Stream-HLS [9] automatically generates dataflow; however, it assumes that data are already on-chip, thereby overlooking communication with off-chip memory. Additionally, it offers very limited opportunities for parallelism. Flower [5] automates FPGA dataflow development but limits parallelism. Frameworks like [15], [74], built on HeteroCL [37], optimize data placement and compute scheduling for heterogeneous systems, maximizing data reuse and bandwidth utilization. Systolic arrays [10], [21], [33], [38], [70] offer efficient computation for specific patterns but lack generalization. Application-specific frameworks [6], [17], [22], [24], [29], [35], [50], [62] demonstrate dataflow advantages but do not generalize across domains. RapidStream-TAPA [27], [28] enhances the performance of dataflow designs and automates SLR placement. However, it requires an optimized kernel with a dataflow structure as input.

Shared Buffer Shared buffer utilization through HLS has been extensively explored using methods such as NLP-based pragma insertion [57]–[59], bottleneck DSE [66], and GNN-based latency and resource estimation [8], [63]–[65], [67], [72], [73]. However, these approaches lack effective integration of dataflow optimization techniques.

Code Transformation Code transformation has been explored for CPUs [7], [14], [36], [54], GPUs [69], and FPGAs [18], [43], [45]–[47], [56], [82], [83]. Pluto [14] minimizes communication and improves locality but can limit parallelism. FPGA-specific adaptations [56] leverage FIFOs for overlapping communication and computation but are restricted in parallelism. Recent works [82], [83] selectively use Pluto for latency minimization while avoiding non-HLS-friendly code. While [18], [43], [45]–[47] focus on optimizing pipelining techniques, they do not address parallelism or the coordination of computation and communication overlap, which are crucial for our objectives. The [15], [31], [37], [77], [78] compilers perform code transformations and pragma insertion, their modifications are primarily heuristic and based on loop properties. The paper [59] described in Section II generates design with high QoR, but the absence of dataflow utilization hinders concurrent task execution. Additionally, their approach avoids padding, limiting the unroll factor to divisors of the loop’s trip count and constraining tiling space.

Tiling and Padding Tiling is essential for balancing computation and communication. While prior works [44], [48] use cost models to minimize communication, our approach extends this to reduce overall latency. Techniques like NLP-based tiling [44] focus on CPUs, while Wedler [60] optimizes DNNs on GPUs by fusing operators, enhancing data reuse, and employing padding to prevent bank conflicts. Padding is well-studied for reducing cache misses [30], [51] and improving memory transfers [71], but its use for varying unroll factors on FPGAs remains underexplored.

VIII. CONCLUSION

In this work, we introduce Prometheus, a comprehensive FPGA performance enhancement framework. By integrating techniques like task fusion, automatic tiling, loop permutation, and overlap of communication and computation, Prometheus is intended to minimize latency within stringent resource constraints. Our methodology utilizes NLP to navigate complex design spaces and automate parameter discovery, achieving superior QoR compared to existing tools.

REFERENCES

- [1] Allo artifact: <https://github.com/cornell-zhang/allo-pldi24-artifact>, 2024.
- [2] Scalehls: <https://github.com/UIUC-ChenLab/scalehls>, 2024.
- [3] Mariem Abid, Khaled Jerbi, Mickaël Raulet, Olivier Déforges, and Mohamed Abid. System level synthesis of dataflow programs: Hevc decoder case study. In *Proceedings of the 2013 Electronic System Level Synthesis Conference (ESLsyn)*, pages 1–6, 2013.
- [4] AMD/Xilinx. *AMD/Xilinx Vitis 2023.2 Documentation*, 2024. Accessed: 2025-01-06.
- [5] Puya Amiri, Arsène Pérard-Gayot, Richard Membarth, Philipp Slusallek, Roland Leißa, and Sebastian Hack. Flower: A comprehensive dataflow compiler for high-level synthesis. In *2021 International Conference on Field-Programmable Technology (ICFPT)*, pages 1–9, 2021.
- [6] Marco Bacis, Giuseppe Natale, Emanuele Del Sozzo, and Marco Domenico Santambrogio. A pipelined and scalable dataflow implementation of convolutional neural networks on fpga. In *2017 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*, pages 90–97, 2017.
- [7] Riyadh Baghdadi, Jessica Ray, Malek Ben Romdhane, Emanuele Del Sozzo, Abdurrahman Akkas, Yunming Zhang, Patricia Suriana, Shoaib Kamil, and Saman Amarasinghe. Tiramisu: A polyhedral compiler for expressing fast and portable code. In *2019 IEEE/ACM International Symposium on Code Generation and Optimization (CGO)*, pages 193–205. IEEE, 2019.
- [8] Yunsheng Bai, Atefeh Sohrabzadeh, Yizhou Sun, and Jason Cong. Improving gnn-based accelerator design automation with meta learning. In *Proceedings of the 59th ACM/IEEE Design Automation Conference, DAC '22*, page 1347–1350, New York, NY, USA, 2022. Association for Computing Machinery.
- [9] Suhail Basalama and Jason Cong. Stream-hls: Towards automatic dataflow acceleration. *arXiv <https://arxiv.org/abs/2501.09118>*, 2025.
- [10] Suhail Basalama, Atefeh Sohrabzadeh, Jie Wang, Licheng Guo, and Jason Cong. Flexcnn: An end-to-end framework for composing cnn accelerators on fpga. *ACM Trans. Reconfigurable Technol. Syst.*, 16(2), mar 2023.
- [11] Tal Ben-Nun, Johannes de Fine Licht, Alexandros N. Ziogas, Timo Schneider, and Torsten Hoefler. Stateful dataflow multigraphs: a data-centric model for performance portability on heterogeneous architectures. In *Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis, SC '19*, New York, NY, USA, 2019. Association for Computing Machinery.
- [12] Albert Benveniste, Paul Caspi, Paul Le Guernic, and Nicolas Halbwachs. Data-flow synchronous languages. In *A Decade of Concurrency Reflections and Perspectives: REX School/Symposium Noordwijkerhout, The Netherlands June 1–4, 1993 Proceedings*, pages 1–45. Springer, 1994.
- [13] Shuvra S. Bhattacharyya, Gordon Brebner, Jörn W. Janneck, Johan Eker, Carl von Platen, Marco Mattavelli, and Mickaël Raulet. Opndf: a dataflow toolset for reconfigurable hardware and multicore systems. *SIGARCH Comput. Archit. News*, 36(5):29–35, jun 2009.
- [14] Uday Bondhugula, Albert Hartono, J. Ramanujam, and P. Sadayappan. A Practical Automatic Polyhedral Parallelizer and Locality Optimizer. In *Proceedings of the 29th ACM SIGPLAN Conference on Programming Language Design and Implementation, PLDI '08*, page 101–113, New York, NY, USA, 2008. Association for Computing Machinery.
- [15] Hongzheng Chen, Niansong Zhang, Shaojie Xiang, Zhichen Zeng, Mengjia Dai, and Zhiru Zhang. Allo: A programming model for composable accelerator design. *Proc. ACM Program. Lang.*, 8(PLDI), jun 2024.
- [16] W.Y. Chen, P.P. Chang, T.M. Conte, and W.W. Hwu. The effect of code expanding optimizations on instruction cache design. *IEEE Transactions on Computers*, 42(9):1045–1057, 1993.
- [17] Yuze Chi, Jason Cong, Peng Wei, and Peipei Zhou. SODA: Stencil with Optimized Dataflow Architecture. In *2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pages 1–8, 2018.
- [18] Young-kyu Choi and Jason Cong. HLS-Based Optimization and Design Space Exploration for Applications with Variable Loop Bounds. In *2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pages 1–8, 2018.
- [19] Jason Cong, Zhenman Fang, Yuchen Hao, Peng Wei, Cody Hao Yu, Chen Zhang, and Peipei Zhou. Best-effort FPGA programming: A few steps can go a long way. *CoRR*, abs/1807.01340, 2018.
- [20] Jason Cong, Bin Liu, Stephen Neuendorffer, Juanjo Noguera, Kees Vissers, and Zhiru Zhang. High-Level Synthesis for FPGAs: From Prototyping to Deployment. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 30(4):473–491, 2011.
- [21] Jason Cong and Jie Wang. Polysa: Polyhedral-based systolic array auto-compilation. In *2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pages 1–8, 2018.
- [22] Johannes de Fine Licht, Andreas Kuster, Tiziano De Matteis, Tal Ben-Nun, Dominic Hofer, and Torsten Hoefler. Stencilflow: Mapping large stencil programs to distributed spatial computing systems. In *2021 IEEE/ACM International Symposium on Code Generation and Optimization (CGO)*, pages 315–326, 2021.
- [23] J. B. Dennis. First version of a data flow procedure language. In *Programming Symposium, Proceedings Colloque Sur La Programmation*, page 362–376, Berlin, Heidelberg, 1974. Springer-Verlag.
- [24] Alain Denzler, Geraldo F. Oliveira, Nastaran Hajinazar, Rahul Bera, Gagandeep Singh, Juan Gómez-Luna, and Onur Mutlu. Casper: Accelerating stencil computations using near-cache processing. *IEEE Access*, 11:22136–22154, 2023.
- [25] Lorenzo Ferretti, Giovanni Ansaloni, and Laura Pozzi. Lattice-Traversing Design Space Exploration for High Level Synthesis. In *2018 IEEE 36th International Conference on Computer Design (ICCD)*, pages 210–217, 2018.
- [26] Paul Grigoras, Xinyu Niu, Jose G. F. Coutinho, Wayne Luk, Jacob Bower, and Oliver Pell. Aspect driven compilation for dataflow designs. In *2013 IEEE 24th International Conference on Application-Specific Systems, Architectures and Processors*, pages 18–25, 2013.
- [27] Licheng Guo, Yuze Chi, Jason Lau, Linghao Song, Xingyu Tian, Moazin Khatti, Weikang Qiao, Jie Wang, Ecenur Ustun, Zhenman Fang, Zhiru Zhang, and Jason Cong. Tapa: A scalable task-parallel dataflow programming framework for modern fpgas with co-optimization of hls and physical design. *ACM Trans. Reconfigurable Technol. Syst.*, 16(4), December 2023.
- [28] Licheng Guo, Pongstorn Maidee, Yun Zhou, Chris Lavin, Eddie Hung, Wuxi Li, Jason Lau, Weikang Qiao, Yuze Chi, Linghao Song, Yuanlong Xiao, Alireza Kaviani, Zhiru Zhang, and Jason Cong. Rapidstream 2.0: Automated parallel implementation of latency-insensitive fpga designs through partial reconfiguration. *ACM Trans. Reconfigurable Technol. Syst.*, 16(4), September 2023.
- [29] James Hegarty, John Brunhaver, Zachary DeVito, Jonathan Ragan-Kelley, Noy Cohen, Steven Bell, Artem Vasilyev, Mark Horowitz, and Pat Hanrahan. Darkroom: compiling high-level image processing code into hardware pipelines. *ACM Trans. Graph.*, 33(4), jul 2014.
- [30] Changwan Hong, Wenlei Bao, Albert Cohen, Sriram Krishnamoorthy, Louis-Noël Pouchet, Fabrice Rastello, J. Ramanujam, and P. Sadayappan. Effective padding of multidimensional arrays to avoid cache conflict misses. *SIGPLAN Not.*, 51(6):129–144, jun 2016.

- [31] Sitao Huang, Kun Wu, Hyunmin Jeong, Chengyue Wang, Deming Chen, and Wen-Mei Hwu. PyLog: An Algorithm-Centric Python-Based FPGA Programming and Synthesis Flow. *IEEE Transactions on Computers*, 70(12):2015–2028, 2021.
- [32] Intel. Intel, 2024.
- [33] Liancheng Jia, Liqiang Lu, Xuechao Wei, and Yun Liang. Generating systolic array accelerators with reusable blocks. *IEEE Micro*, 40(4):85–92, 2020.
- [34] Gilles Kahn. The semantics of a simple language for parallel programming. In Jack L. Rosenfeld, editor, *Information Processing, Proceedings of the 6th IFIP Congress 1974, Stockholm, Sweden, August 5-10, 1974*, pages 471–475. North-Holland, 1974.
- [35] Guilherme Korol, Michael Guilherme Jordan, Mateus Beck Rutzig, and Antonio Carlos Schneider Beck. AdafLOW: A framework for adaptive dataflow CNN acceleration on FPGAs. In *2022 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 244–249, 2022.
- [36] Michael Kruse, Hal Finkel, and Xingfu Wu. Autotuning search space for loop transformations. In *2020 IEEE/ACM 6th Workshop on the LLVM Compiler Infrastructure in HPC (LLVM-HPC) and Workshop on Hierarchical Parallelism for Exascale Computing (HiPar)*, pages 12–22. IEEE, 2020.
- [37] Yi-Hsiang Lai, Yuze Chi, Yuwei Hu, Jie Wang, Cody Hao Yu, Yuan Zhou, Jason Cong, and Zhiru Zhang. HeteroCL: A Multi-Paradigm Programming Infrastructure for Software-Defined Reconfigurable Computing. In *Proceedings of the 2019 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, FPGA '19*, page 242–251, New York, NY, USA, 2019. Association for Computing Machinery.
- [38] Yi-Hsiang Lai, Hongbo Rong, Size Zheng, Weihao Zhang, Xiuping Cui, Yunshan Jia, Jie Wang, Brendan Sullivan, Zhiru Zhang, Yun Liang, Youhui Zhang, Jason Cong, Nithin George, Jose Alvarez, Christopher Hughes, and Pradeep Dubey. Susy: a programming model for productive construction of high-performance systolic arrays on FPGAs. In *Proceedings of the 39th International Conference on Computer-Aided Design, ICCAD '20*, New York, NY, USA, 2020. Association for Computing Machinery.
- [39] Chris Lattner, Mehdi Amini, Uday Bondhugula, Albert Cohen, Andy Davis, Jacques Pienaar, River Riddle, Tatiana Shpeisman, Nicolas Vasilache, and Oleksandr Zinenko. MLIR: Scaling compiler infrastructure for domain specific computation. In *2021 IEEE/ACM International Symposium on Code Generation and Optimization (CGO)*, pages 2–14, 2021.
- [40] E.A. Lee and T.M. Parks. Dataflow process networks. *Proceedings of the IEEE*, 83(5):773–801, 1995.
- [41] Edward Ashford Lee and David G. Messerschmitt. Static scheduling of synchronous data flow programs for digital signal processing. *IEEE Transactions on Computers*, C-36(1):24–35, 1987.
- [42] Jiajie Li, Yuze Chi, and Jason Cong. HeteroHalide: From Image Processing DSL to Efficient FPGA Acceleration. In *Proceedings of the 2020 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, FPGA '20*, page 51–57, New York, NY, USA, 2020. Association for Computing Machinery.
- [43] Peng Li, Louis-Noël Pouchet, and Jason Cong. Throughput optimization for high-level synthesis using resource constraints. In *Int. Workshop on Polyhedral Compilation Techniques (IMPACT'14)*, 2014.
- [44] Rui Li, Yufan Xu, Aravind Sukumaran-Rajam, Atanas Rountev, and P. Sadayappan. Analytical characterization and design space exploration for optimization of CNNs. In *Proceedings of the 26th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, ASPLOS '21*, page 928–942, New York, NY, USA, 2021. Association for Computing Machinery.
- [45] Junyi Liu, Samuel Bayliss, and George A. Constantinides. Offline Synthesis of Online Dependence Testing: Parametric Loop Pipelining for HLS. In *2015 IEEE 23rd Annual International Symposium on Field-Programmable Custom Computing Machines*, pages 159–162, 2015.
- [46] Junyi Liu, John Wickerson, Samuel Bayliss, and George A. Constantinides. Polyhedral-based dynamic loop pipelining for high-level synthesis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 37(9):1802–1815, 2017.
- [47] Junyi Liu, John Wickerson, and George A. Constantinides. Loop splitting for efficient pipelining in high-level synthesis. In *2016 IEEE 24th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pages 72–79. IEEE, 2016.
- [48] Junyi Liu, John Wickerson, and George A. Constantinides. Tile size selection for optimized memory reuse in high-level synthesis. In *2017 27th International Conference on Field Programmable Logic and Applications (FPL)*, pages 1–8, 2017.
- [49] Microchip. SmartHLS Compiler Software, 2023.
- [50] Giuseppe Natale, Giulio Stramondo, Pietro Bressana, Riccardo Cattaneo, Donatella Sciuto, and Marco D. Santambrogio. A polyhedral model-based framework for dataflow implementation on FPGA devices of iterative stencil loops. In *2016 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pages 1–8, 2016.
- [51] P.R. Panda, H. Nakamura, N.D. Dutt, and A. Nicolau. Augmenting loop tiling with data alignment for improved cache performance. *IEEE Transactions on Computers*, 48(2):142–149, 1999.
- [52] Francesco Peverelli, Marco Rabozzi, Emanuele Del Sozzo, and Marco D. Santambrogio. Oxigen: A tool for automatic acceleration of C functions into dataflow FPGA-based kernels. In *2018 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*, pages 91–98, 2018.
- [53] PoCC, the Polyhedral Compiler Collection 1.3.
- [54] Louis-Noël Pouchet, Uday Bondhugula, Cédric Bastoul, Albert Cohen, J. Ramanujam, P. Sadayappan, and Nicolas Vasilache. Loop transformations: Convexity, pruning and optimization. In *Proceedings of the 38th Annual ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages, POPL '11*, pages 549–562, New York, NY, USA, 2011. ACM.
- [55] Louis-Noël Pouchet and Tomofumi Yuki. Polybench: The polyhedral benchmark suite, Retrieved 2024.
- [56] Louis-Noël Pouchet, Peng Zhang, P. Sadayappan, and Jason Cong. Polyhedral-Based Data Reuse Optimization for Configurable Computing. In *Proceedings of the ACM/SIGDA International Symposium on Field Programmable Gate Arrays, FPGA '13*, page 29–38, New York, NY, USA, 2013. Association for Computing Machinery.
- [57] Stéphane Pouget, Louis-Noël Pouchet, and Jason Cong. Automatic hardware pragma insertion in high-level synthesis: A non-linear programming approach. In *Proceedings of the 2024 ACM/SIGDA International Symposium on Field Programmable Gate Arrays, FPGA '24*, page 184, New York, NY, USA, 2024. Association for Computing Machinery.
- [58] Stéphane Pouget, Louis-Noël Pouchet, and Jason Cong. Automatic hardware pragma insertion in high-level synthesis: A non-linear programming approach. *ACM Trans. Des. Autom. Electron. Syst.*, January 2025. Just Accepted.
- [59] Stéphane Pouget, Louis-Noël Pouchet, and Jason Cong. A unified framework for automated code transformation and pragma insertion. *arXiv <https://arxiv.org/abs/2405.03058>*, 2025.
- [60] Yining Shi, Zhi Yang, Jilong Xue, Lingxiao Ma, Yuqing Xia, Ziming Miao, Yuxiao Guo, Fan Yang, and Lidong Zhou. Welder: Scheduling deep learning memory access via tile-graph. In *17th USENIX Symposium on Operating Systems Design and Implementation (OSDI 23)*, pages 701–718, Boston, MA, July 2023. USENIX Association.
- [61] Siemens. Catapult High-Level Synthesis, 2023.
- [62] Gagandeep Singh, Dionysios Diamantopoulos, Christoph Hagleitner, Juan Gomez-Luna, Sander Stuijk, Onur Mutlu, and Henk Corporaal. Nero: A near high-bandwidth memory stencil accelerator for weather prediction modeling. In *2020 30th International Conference on Field-Programmable Logic and Applications (FPL)*, pages 9–17, 2020.
- [63] Atefeh Sohrabzadeh, Yunsheng Bai, Yizhou Sun, and Jason Cong. Automated Accelerator Optimization Aided by Graph Neural Networks. In *2022 59th ACM/IEEE Design Automation Conference (DAC)*, 2022.
- [64] Atefeh Sohrabzadeh, Yunsheng Bai, Yizhou Sun, and Jason Cong. Automated accelerator optimization aided by graph neural networks. In *Proceedings of the 59th ACM/IEEE Design Automation Conference, DAC '22*, page 55–60, New York, NY, USA, 2022. Association for Computing Machinery.
- [65] Atefeh Sohrabzadeh, Yunsheng Bai, Yizhou Sun, and Jason Cong. Robust gnn-based representation learning for HLS. In *2023 IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, pages 1–9, 2023.
- [66] Atefeh Sohrabzadeh, Cody Hao Yu, Min Gao, and Jason Cong. AutoDSE: Enabling Software Programmers Design Efficient FPGA Accelerators. In *The 2021 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, FPGA '21*, page 147, New York, NY, USA, 2021. Association for Computing Machinery.
- [67] Ecenur Ustun, Chenhui Deng, Debjit Pal, Zhijing Li, and Zhiru Zhang. Accurate operation delay prediction for FPGA HLS using graph neural networks. In *2020 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, pages 1–9, 2020.

- [68] Sven Verdoolaege. Counting affine calculator and applications. In *First International Workshop on Polyhedral Compilation Techniques (IMPACT'11)*, Chamonix, France, 2011.
- [69] Sven Verdoolaege, Juan Carlos Juega, Albert Cohen, José Ignacio Gómez, Christian Tenllado, and Francky Catthoor. Polyhedral parallel code generation for cuda. *ACM Trans. Archit. Code Optim.*, 9(4), jan 2013.
- [70] Jie Wang, Licheng Guo, and Jason Cong. AutoSA: A Polyhedral Compiler for High-Performance Systolic Arrays on FPGA. In *The 2021 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, FPGA '21, page 93–104, New York, NY, USA, 2021. Association for Computing Machinery.
- [71] Yuxin Wang, Peng Zhang, Xu Cheng, and Jason Cong. An integrated and automated memory optimization flow for fpga behavioral synthesis. In *17th Asia and South Pacific Design Automation Conference*, pages 257–262, 2012.
- [72] Nan Wu, Yuan Xie, and Cong Hao. IronMan-Pro: Multi-objective Design Space Exploration in HLS via Reinforcement Learning and Graph Neural Network based Modeling. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pages 1–1, 2022.
- [73] Nan Wu, Hang Yang, Yuan Xie, Pan Li, and Cong Hao. High-level synthesis performance prediction using gnns: benchmarking, modeling, and advancing. In *Proceedings of the 59th ACM/IEEE Design Automation Conference*, DAC '22, page 49–54, New York, NY, USA, 2022. Association for Computing Machinery.
- [74] Shaojie Xiang, Yi-Hsiang Lai, Yuan Zhou, Hongzheng Chen, Niansong Zhang, Debjit Pal, and Zhiru Zhang. Heteroflow: An accelerator programming model with decoupled data placement for software-defined fpgas. In *Proceedings of the 2022 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, FPGA '22, page 78–88, New York, NY, USA, 2022. Association for Computing Machinery.
- [75] AMD Xilinx. Vitis, 2023.2.
- [76] AMD Xilinx. Merlin: <https://github.com/Xilinx/merlin-compiler>, 2024.
- [77] Hanchen Ye, HyeGang Jun, and Deming Chen. Hida: A hierarchical dataflow compiler for high-level synthesis. In *Proceedings of the 29th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 1*, ASPLOS '24, page 215–230, New York, NY, USA, 2024. Association for Computing Machinery.
- [78] Hanchen Ye, HyeGang Jun, Hyunmin Jeong, Stephen Neuendorffer, and Deming Chen. ScaleHLS: A Scalable High-Level Synthesis Framework with Multi-Level Transformations and Optimizations: Invited. In *Proceedings of the 59th ACM/IEEE Design Automation Conference*, DAC '22, page 1355–1358, New York, NY, USA, 2022. Association for Computing Machinery.
- [79] Cody Hao Yu, Peng Wei, Max Grossman, Peng Zhang, Vivek Sarker, and Jason Cong. S2FA: An Accelerator Automation Framework for Heterogeneous Computing in Datacenters. In *2018 55th ACM/ESDA/IEEE Design Automation Conference (DAC)*, pages 1–6, 2018.
- [80] Zhiru Zhang, Yiping Fan, Wei Jiang, Guoling Han, Changqi Yang, and Jason Cong. *AutoPilot: A Platform-Based ESL Synthesis System*, pages 99–112. Springer Netherlands, Dordrecht, 2008.
- [81] Jieru Zhao, Liang Feng, Sharad Sinha, Wei Zhang, Yun Liang, and Bingsheng He. COMBA: A comprehensive model-based analysis framework for high level synthesis of real applications. In *2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pages 430–437, 2017.
- [82] Ruizhe Zhao and Jianyi Cheng. Phism: Polyhedral High-Level Synthesis in MLIR. *arXiv preprint arXiv:2103.15103*, 2021.
- [83] Ruizhe Zhao, Jianyi Cheng, Wayne Luk, and George A Constantinides. POLSCA: Polyhedral High-Level Synthesis with Compiler Transformations. *arXiv*, 2022.